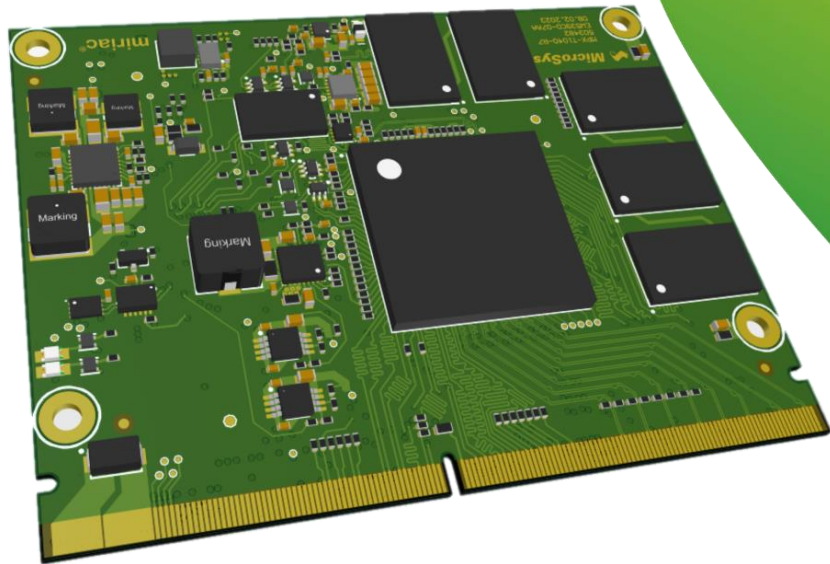




miriac MPX-T1042

User Manual (HW Revision 7)

V 7.0

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1 General Notes

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1.5 Symbols, Conventions and Abbreviations

1.5.1 Symbols

Throughout this document, the following symbols will be used:



Information marked with this symbol **MUST** be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment



Information marked with this symbol **MUST** be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.



Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features.

Table 1-1 Symbols

1.5.2 Conventions

Symbol	explanation
#	denotes a low active signal
←	denotes the signal flow in the shown direction
→	denotes the signal flow in the shown direction
↔	denotes the signal flow in both directions
→	denotes the signal flow in the shown direction with additional logic / additional ICs in the signal path
I/O	denotes a bidirectional pin
Input	denotes an input pin
matched	denotes the according signal to be routed impedance controlled and length matched
Output	denotes an output pin
Pin 1	refers to the numeric pin of a component package
Pin a1	refers to the array position of a pin within a component package
XXX-	denotes the negative signal of a differential pair
XXX+	denotes the positive signal of a differential pair
XXX	denotes an optional not mounted or fitted part

Table 1-2 Conventions

1.6 Safety and Handling Precautions



DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.

ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.



Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns, and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.



ALWAYS take care of ESD-safe handling!

Many pins on the module connector are directly connected to the CPU or other ESD sensitive devices.

Make or break **ANY** connections **ONLY** while the unit is switched OFF.

Otherwise, permanent damage to the unit may occur, which is not covered by warranty.



There is no separate SHIELD connection.

The module's mounting holes are not connected to GND. Take this into account when handling and mounting the unit.

Table 1-3 Safety and Handling Precautions

2 Short Description

The miriac MPX-T1042 is a member of the MPX module family based on the MicroSys MPX2 specification and NXP's QorIQ® Power Architecture T1042 Multicore Communications Processor.

MicroSys Electronics GmbH offers a Starterkit which provides the key features of the module. The customer can:

- ...evaluate the basic concept of the MPX2 standard
- ...test the operation of the MPX-T1042 module
- ...evaluate the main interfaces of the T1042 CPU
- ...test the provided software
- ...start developing

3 System Description

3.1 Block Diagram

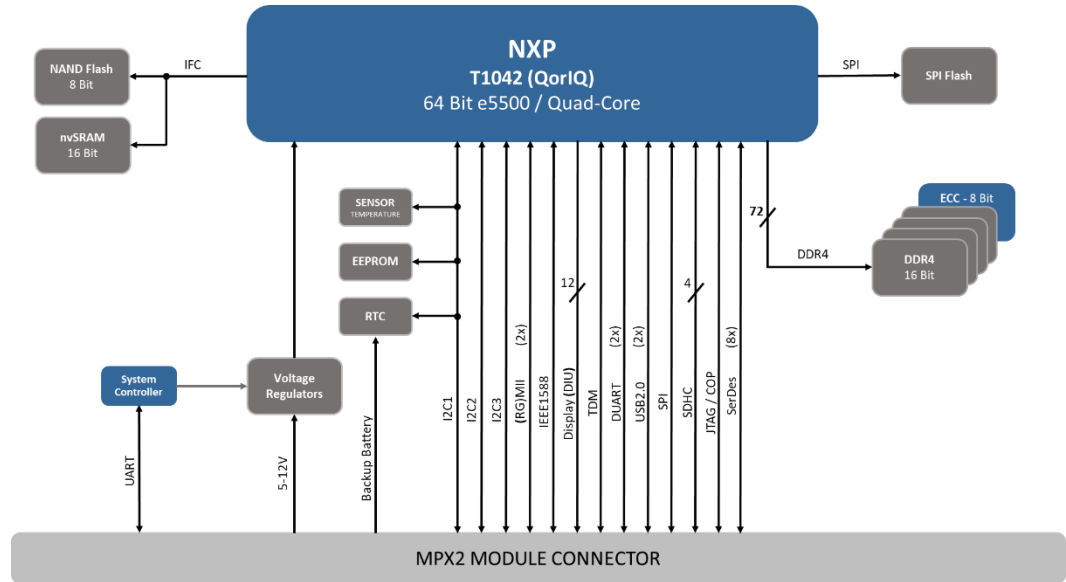


Figure 3-1 Block Diagram

3.2 System Components

- QorIQ Power Architecture processor T1042 or T1022
- Microcontroller as monitoring and supervising unit with power management and configuration tasks
- DDR4 SDRAM
- Clock Generators for CPU and interface clocks
- SPI flash as boot or storage device
- NAND flash as boot or storage device
- nvSRAM
- I²C EEPROM
- I²C temperature sensor
- I²C RTC
- Voltage regulators for onboard generated voltages

3.3 Power Consumption

The MPX-T1042 can be supplied by a single input power rail ranging from 5V to 12V. The efficiency of the voltage regulators differs in that range. Thus, for best overall efficiency choose 5V input voltage if possible. The typical power consumption values for the module are determined on a CRX05 carrier board running U-boot (idle) at room temperature (4 cores @ 1200MHz / 500MHz CCB clock) with 2GByte of DDR4 memory + ECC (1600 MHz) and passive cooling:

- 5V input: ~7,2 Watt
- 12V input: ~7,7 Watt

The consumed power is distributed among the following components based on estimated values:

- CPU: ~5-7 Watt
- DDR4 + ECC: ~1-1,5 Watt
- SPI Flash: ~0,05 Watt
- NAND Flash: ~0,05 Watt
- Onboard clock generator: ~0,25 Watt
- Temperature Sensor, RTC, EEPROM: ~0,025 Watt
- Regulator efficiency: ~80-90%

3.4 Cooling

In chapter 3.3 the power consumption of the MPX-T1042 module was specified. With this information a cooling method needs to be designed in coordination with the final use case. If desired, MicroSys Electronics GmbH can support you with your cooling concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Commercial temperature grade (0/+70° C) variants:

Component	Temperature (max.)	Description
CPU	105° C	Junction Temperature
DDR	85° C	Case Temperature
Core Regulator	150° C	Junction Temperature

Table 3-1 Commercial grade variants: maximum temperature

Industrial temperature grade (-40/+85° C) variants:

Component	Temperature (max.)	Description
CPU	105° C	Junction Temperature
DDR	95° C	Case Temperature
Core Regulator	150° C	Junction Temperature

Table 3-2 Industrial grade variants: maximum temperature

3.5 **Ordering Information**

Ordering information can be found on the website

<https://www.microsys.de/en/products/system-on-modules/power-architecture/miriac-mpx-t1042-som/>

or contact your local sales representative.

4 Technical Description

4.1 Pinouts



The signal direction is from the module's view. For example JTDO (pin B104) is an output from the module and an input to peripheral devices on the carrier board.

The following table gives an overview of the 314 pins of the module's edge finger. For a detailed connector description see chapter 5.1. The pins will be described in chapter 4.10 and the following sections.

4.1.1 Module Connector – Bottom Pins [ST1]



The following pinout is specific for the MPX-T1042 module and to large parts common for most of the MPX modules.

Nevertheless, different modules do not claim to be pin compatible. Individual modules may have deviating assignments for some functions, whereas power and ground are always assigned to the same pins.

Pin	Signal	I/O	Group	Power Rail
B1	n.c.	O	Quicc Engine	3,3V Level
B2	GND		Power	Ground
B3	n.c.	I/O	Quicc Engine	3,3V Level
B4	n.c.	I/O	Quicc Engine	3,3V Level
B5	n.c.	I/O	Quicc Engine	3,3V Level
B6	n.c.	I/O	Quicc Engine	3,3V Level
B7	n.c.	I/O	Quicc Engine	3,3V Level
B8	GND		Power	Ground
B9	n.c.	I/O	Quicc Engine	3,3V Level
BK1	n.c.			
BK2	n.c.			
B10	n.c.	I/O	Quicc Engine	3,3V Level
B11	n.c.	I/O	Quicc Engine	3,3V Level
B12	GPIO-E14	I/O	GPIO	1,8V Level
B13	n.c.	I/O	Quicc Engine	3,3V Level
B14	GND		Power	Ground

Pin	Signal	I/O	Group	Power Rail
B15	GPIO-C15	I/O	GPIO	1,8V Level
B16	GPIO-C14	I/O	GPIO	1,8V Level
B17	GND		Power	Ground
B18	GPIO-D18	I/O	GPIO	1,8V Level
B19	GPIO-C19	I/O	GPIO	1,8V Level
B20	GND		Power	Ground
B21	I2C3-SCL	O	I2C	3,3V Level
B22	I2C3-SDA	I/O	I2C	3,3V Level
B23	GND		Power	Ground
B24	TDM-RFS	I/O	TDM / DMA	3,3V Level
B25	TDM-RXD	I/O	TDM / DMA	3,3V Level
B26	TDM-TFS	I/O	TDM / DMA	3,3V Level
B27	TDM-TXD	I/O	TDM / DMA	3,3V Level
B28	GND		Power	Ground
B29	TDM-RCK	I	TDM / DMA	3,3V Level
B30	TDM-TCK	O	TDM / DMA	3,3V Level
B31	GND		Power	Ground
B32	UART2-RXD	I	UART2	3,3V Level
B33	UART2-TXD	O	UART2	3,3V Level
B34	UART2-CTS#	I	UART2	3,3V Level
B35	UART2-RTS#	O	UART2	3,3V Level
B36	GND		Power	Ground
B37	UART1-RXD	I	UART	3,3V Level
B38	UART1-TXD	O	UART	3,3V Level
B39	UART1-CTS#	I	UART	3,3V Level
B40	UART1-RTS#	O	UART	3,3V Level
B41	GND		Power	Ground
B42	1588-CLKO	O	IEEE1588	1,8V Level
B43	1588-CLKI	I	IEEE1588	1,8V Level
B44	1588-PLSO2	O	IEEE1588	1,8V Level
B45	1588-PLSO1	O	IEEE1588	1,8V Level

Pin	Signal	I/O	Group	Power Rail
B46	1588-TRGI2	I	IEEE1588	1,8V Level
B47	1588-TRGI1	I	IEEE1588	1,8V Level
B48	1588-ALRO2	O	IEEE1588	1,8V Level
B49	1588-ALRO1	O	IEEE1588	1,8V Level
B50	GND		Power	Ground
B51	DIU-HSN	O	Display	3,3V Level
B52	DIU-VSN	O	Display	3,3V Level
B53	DIU-DE	O	Display	3,3V Level
B54	DIU-CLK	O	Display	3,3V Level
B55	GND		Power	Ground
B56	DIU-D11	O	Display	3,3V Level
B57	DIU-D10	O	Display	3,3V Level
B58	DIU-D9	O	Display	3,3V Level
B59	DIU-D8	O	Display	3,3V Level
B60	DIU-D7	O	Display	3,3V Level
B61	DIU-D6	O	Display	3,3V Level
B62	DIU-D5	O	Display	3,3V Level
B63	DIU-D4	O	Display	3,3V Level
B64	DIU-D3	O	Display	3,3V Level
B65	DIU-D2	O	Display	3,3V Level
B66	DIU-D1	O	Display	3,3V Level
B67	DIU-D0	O	Display	3,3V Level
B68	GND		Power	Ground
B69	SPI-CLK	O	SPI	3,3V Level
B70	SPI-CS0#	O	SPI	3,3V Level
B71	SPI-MOSI	O	SPI	3,3V Level
B72	SPI-MISO	I	SPI	3,3V Level
B73	GND		Power	Ground
B74	I2C2-SDA	I/O	I2C	3,3V Level
B75	I2C2-SCL	O	I2C	3,3V Level
B76	GND		Power	Ground

Pin	Signal	I/O	Group	Power Rail
B77	I2C1-SDA	I/O	I2C	3,3V Level
B78	I2C1-SCL	O	I2C	3,3V Level
B79	GND		Power	Ground
B80	VBAT	Power	Power	3,0V
B81	VREF-SDC	Power	Power	Reference voltage for SD-Card Interface
B82	GND		Power	Ground
B83	n.c.	O	EC Management2	1,2V Level
B84	n.c.	I/O	EC Management2	1,2V Level
B85	GND		Power	Ground
B86	MDC1	O	EC Management1	VREF-MII
B87	MDIO1	I/O	EC Management1	VREF-MII
B88	GND		Power	Ground
B89	SDC-WP	O	SDHC	VREF-SDC
B90	SDC-CD#	I	SDHC	VREF-SDC
B91	SDC-D7 / SPI-CS3#	I/O	SDHC / SPI	VREF-SDC
B92	SDC-D6 / SPI-CS2#	I/O	SDHC / SPI	VREF-SDC
B93	SDC-D5 / SPI-CS1#	I/O	SDHC / SPI	VREF-SDC
B94	SDC-D4 / SPI-CS0#	I/O	SDHC / SPI	VREF-SDC
B95	SDC-D3	I/O	SDHC	VREF-SDC
B96	SDC-D2	I/O	SDHC	VREF-SDC
B97	SDC-D1	I/O	SDHC	VREF-SDC
B98	SDC-D0	I/O	SDHC	VREF-SDC
B99	SDC-CMD	I/O	SDHC	VREF-SDC
B100	SDC-CLK	O	SDHC	VREF-SDC
B101	GND		Power	Ground
B102	JTMS	I	JTAG	1,8V Level
B103	JTDI	I	JTAG	1,8V Level
B104	JTDO	O	JTAG	1,8V Level
B105	JTCK	I	JTAG	1,8V Level
B106	COP-TRST#	O	JTAG / COP	1,8V Level
B107	GND		Power	

Pin	Signal	I/O	Group	Power Rail
B108	n.c.	I	COP	1,8V Level
B109	COP-CKSTPO#	O	COP	1,8V Level
B110	COP-PRST#	O	COP	1,8V Level
B111	COP-HRST#	O	COP	1,8V Level
B112	GND		Power	Ground
B113	DBG-RXD	I	Debug	1,8V Level
B114	DBG-TXD	O	Debug	1,8V Level
B115	GND		Power	Ground
B116	GPIO1	I/O	GPIO	1,8V Level
B117	GPIO2	I/O	GPIO	1,8V Level
B118	GPIO3 / WDOG-TRIG#	I/O	GPIO	1,8V Level
B119	GPIO4	I/O	GPIO	1,8V Level
B120	GPIO5	I/O	GPIO	1,8V Level
B121	GPIO6	I/O	GPIO	1,8V Level
B122	GPIO7	I/O	GPIO	1,8V Level
B123	GPIO8	I/O	GPIO	1,8V Level
B124	GND		Power	Ground
B125	USB2-ID	Analog	USB2.0	1,8V Level
B126	USB2-OC	I	USB2.0	3,3V Level
B127	USB2-EN	O	USB2.0	3,3V Level
B128	USB2-VBUS	I	USB2.0	5V sense
B129	GND		Power	Ground
B130	USB1-ID	Analog	USB2.0	1,8V Level
B131	USB1-OC	I	USB2.0	3,3V Level
B132	USB1-EN	O	USB2.0	3,3V Level
B133	USB1-VBUS	I	USB2.0	5V sense
B134	GND		Power	Ground
B135	n.c.	Analog	USB2.0	1,8V Level
B136	n.c.	I	USB2.0	3,3V Level
B137	n.c.	O	USB2.0	3,3V Level
B138	n.c.	I	USB2.0	5V sense

Pin	Signal	I/O	Group	Power Rail
B139	GND		Power	Ground
B140	GND		Power	Ground
B141	GND		Power	Ground
B142	GND		Power	Ground
B143	GND		Power	Ground
B144	GND		Power	Ground
B145	GND		Power	Ground
B146	GND		Power	Ground
B147	GND		Power	Ground
B148	VCC		Power	5V (-5%) up to 12V (+5%)
B149	VCC		Power	5V (-5%) up to 12V (+5%)
B150	VCC		Power	5V (-5%) up to 12V (+5%)
B151	VCC		Power	5V (-5%) up to 12V (+5%)
B152	VCC		Power	5V (-5%) up to 12V (+5%)
B153	VCC		Power	5V (-5%) up to 12V (+5%)
B154	VCC		Power	5V (-5%) up to 12V (+5%)
B155	VCC		Power	5V (-5%) up to 12V (+5%)
B156	VCC		Power	5V (-5%) up to 12V (+5%)

Table 4-1 Module connector: Bottom pins

4.1.2 Module Connector – Top Pins [ST1]



The following pinout is specific for the MPX-T1042 module and to large parts common for most of the MPX modules.

Nevertheless, different modules do not claim to be pin compatible. Individual modules may have deviating assignments for some functions, whereas power and ground are always assigned to the same pins.

Pin	Signal	I/O	Group	Power Rail
T1	GND		Power	Ground
T2	RX7+	I	Serdes	
T3	RX7-	I	Serdes	
T4	GND		Power	Ground
T5	TX7+	O	Serdes	
T6	TX7-	O	Serdes	
T7	GND		Power	Ground
T8	RX6+	I	Serdes	
T9	RX6-	I	Serdes	
TK1				
TK2	VCC-PROG-SFP		Power	
T10	GND		Power	Ground
T11	TX6+	O	Serdes	
T12	TX6-	O	Serdes	
T13	GND		Power	Ground
T14	RX5+	I	Serdes	
T15	RX5-	I	Serdes	
T16	GND		Power	Ground
T17	TX5+	O	Serdes	
T18	TX5-	O	Serdes	
T19	GND		Power	Ground
T20	RX4+	I	Serdes	
T21	RX4-	I	Serdes	
T22	GND		Power	Ground
T23	TX4+	O	Serdes	
T24	TX4-	O	Serdes	
T25	GND		Power	Ground
T26	RX3+	I	Serdes	
T27	RX3-	I	Serdes	

Pin	Signal	I/O	Group	Power Rail
T28	GND		Power	Ground
T29	TX3+	O	Serdes	
T30	TX3-	O	Serdes	
T31	GND		Power	Ground
T32	RX2+	I	Serdes	
T33	RX2-	I	Serdes	
T34	GND		Power	Ground
T35	TX2+	O	Serdes	
T36	TX2-	O	Serdes	
T37	GND		Power	Ground
T38	RX1+	I	Serdes	
T39	RX1-	I	Serdes	
T40	GND		Power	Ground
T41	TX1+	O	Serdes	
T42	TX1-	O	Serdes	
T43	GND		Power	Ground
T44	RX0+	I	Serdes	
T45	RX0-	I	Serdes	
T46	GND		Power	Ground
T47	TX0+	O	Serdes	
T48	TX0-	O	Serdes	
T49	GND		Power	Ground
T50	CLK1+	O	Serdes	
T51	CLK1-	O	Serdes	
T52	GND		Power	Ground
T53	CLK2+	O	Serdes	
T54	CLK2-	O	Serdes	
T55	GND		Power	Ground
T56	MII2-TXEN [TXCTL]	O	MII [RGMII2]	VREF-MII
T57	n.c.	I/O	Serdes / MII [RGMII2]	VREF-MII
T58	GND		Power	Ground
T59	MII2-TXD0 [TXD0]	O	MII [RGMII2]	VREF-MII
T60	MII2-TXD1 [TXD1]	O	MII [RGMII2]	VREF-MII
T61	GND		Power	Ground
T62	MII2-TXD2 [TXD2]	O	MII [RGMII2]	VREF-MII
T63	MII2-TXD3 [TXD3]	O	MII [RGMII2]	VREF-MII

Pin	Signal	I/O	Group	Power Rail
T64	GND		Power	Ground
T65	MII2-TCLK [TCLK]	O	MII [RGMII2]	VREF-MII
T66	MII2-RXDV [RXCTL]	I	MII [RGMII2]	VREF-MII
T67	GND		Power	Ground
T68	MII2-RXD0 [RXD0]	I	MII [RGMII2]	VREF-MII
T69	MII2-RXD1 [RXD1]	I	MII [RGMII2]	VREF-MII
T70	GND		Power	Ground
T71	MII2-RXD2 [RXD2]	I	MII [RGMII2]	VREF-MII
T72	MII2-RXD3 [RXD3]	I	MII [RGMII2]	VREF-MII
T73	GND		Power	Ground
T74	n.c.	I	Serdes / MII [RGMII2]	VREF-MII
T75	MII2-RCLK [RCLK]	I	MII [RGMII2]	VREF-MII
T76	GND		Power	Ground
T77	MII2-COL [CLK125M]	I	MII [RGMII2]	VREF-MII
T78	n.c.	O/I	MII [RGMII2]	VREF-MII
T79	GND		Power	Ground
T80	VREF-MII		Power	Reference Voltage for MII-Interface
T81	GND		Power	Ground
T82	MII-COL [--]	I	MII [RGMII1]	VREF-MII
T83	MII-CRS [CLK125M]	I	MII [RGMII1]	VREF-MII
T84	GND		Power	Ground
T85	MII-RXER [--]	I	MII [RGMII1]	VREF-MII
T86	MII-RCLK [RCLK]	I	MII [RGMII1]	VREF-MII
T87	GND		Power	Ground
T88	MII-RXD0 [RXD0]	I	MII [RGMII1]	VREF-MII
T89	MII-RXD1 [RXD1]	I	MII [RGMII1]	VREF-MII
T90	GND		Power	Ground
T91	MII-RXD2 [RXD2]	I	MII [RGMII1]	VREF-MII
T92	MII-RXD3 [RXD3]	I	MII [RGMII1]	VREF-MII
T93	GND		Power	Ground
T94	MII-TCLK [TCLK]	O	MII [RGMII1]	VREF-MII
T95	MII-RXDV [RXCTL]	I	MII [RGMII1]	VREF-MII
T96	GND		Power	Ground
T97	MII-TXD0 [TXD0]	O	MII [RGMII1]	VREF-MII
T98	MII-TXD1 [TXD1]	O	MII [RGMII1]	VREF-MII
T99	GND		Power	Ground

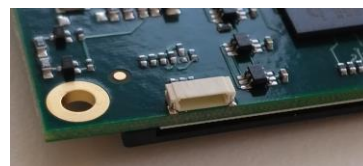
Pin	Signal	I/O	Group	Power Rail
T100	MII-TXD2 [TXD2]	O	MII [RGMII1]	VREF-MII
T101	MII-TXD3 [TXD3]	O	MII [RGMII1]	VREF-MII
T102	GND		Power	Ground
T103	MII-TXEN [TXCTL]	O	MII [RGMII1]	VREF-MII
T104	n.c.	O	MII [RGMII1]	VREF-MII
T105	GND		Power	Ground
T106	n.c.	I	USB3.0	
T107	n.c.	I	USB3.0	
T108	GND		Power	Ground
T109	n.c.	O	USB3.0	
T110	n.c.	O	USB3.0	
T111	GND		Power	Ground
T112	n.c.	I	USB3.0	
T113	n.c.	I	USB3.0	
T114	GND		Power	Ground
T115	n.c.	O	USB3.0	
T116	n.c.	O	USB3.0	
T117	GND		Power	Ground
T118	n.c.	I	USB3.0	
T119	n.c.	I	USB3.0	
T120	GND		Power	Ground
T121	n.c.	O	USB3.0	
T122	n.c.	O	USB3.0	
T123	GND		Power	Ground
T124	n.c.	I/O	USB2.0 Port3	
T125	n.c.	I/O	USB2.0 Port3	
T126	GND		Power	Ground
T127	USB2_D+	I/O	USB2.0 Port2	
T128	USB2_D-	I/O	USB2.0 Port2	
T129	GND		Power	Ground
T130	USB1_D+	I/O	USB2.0 Port1	
T131	USB1_D-	I/O	USB2.0 Port1	
T132	GND		Power	Ground
T133	BOOT-SEL2	I	Management	1,8V Level
T134	BOOT-SEL1	I	Management	1,8V Level
T135	RST-OUT#	O	Management	Open collector output

Pin	Signal	I/O	Group	Power Rail
T136	RST-IN#	I	Management	
T137	GND		Power	Ground
T138	GND		Power	Ground
T139	GND		Power	Ground
T140	GND		Power	Ground
T141	GND		Power	Ground
T142	GND		Power	Ground
T143	GND		Power	Ground
T144	GND		Power	Ground
T145	GND		Power	Ground
T146	VCC		Power	5V (-5%) up to 12V (+5%)
T147	VCC		Power	5V (-5%) up to 12V (+5%)
T148	VCC		Power	5V (-5%) up to 12V (+5%)
T149	VCC		Power	5V (-5%) up to 12V (+5%)
T150	VCC		Power	5V (-5%) up to 12V (+5%)
T151	VCC		Power	5V (-5%) up to 12V (+5%)
T152	VCC		Power	5V (-5%) up to 12V (+5%)
T153	VCC		Power	5V (-5%) up to 12V (+5%)
T154	VCC		Power	5V (-5%) up to 12V (+5%)

Table 4-2 Module connector: top pins

4.1.3 Aurora Connector [ST4]

Manufacturer:	JST
Type:	SM06B-XSRS-ETB
Mates with:	06XSR-36S



CPU		→	ST4			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
D6	EVT0#		1	HALT#	1,8V	PU: 4,7k
C4	EVT1#		2	EVTI#	1,8V	PU: 4,7k
C3	EVT4#		3	EVTO#	1,8V	PU: 4,7k
			4	-		
			5	-		
			6	-		

Table 4-3 Aurora Connector: Pinout and pin assignments

4.1.4 Programming Connector [ST3]

Manufacturer:	JST
Type:	SM06B-XSRS-ETB
Mates with:	06XSR-36S



CPU	
Ball	Signal
F12	PROG_SFP

ST3			
Pin	Signal	I/O Range	Signal conditioning
1	1,8V Supply	1,8V	
2	PROG-SFP	1,8V	PD: 330R
3	t.b.d.		For production use only – do not connect
4	t.b.d.		For production use only – do not connect
5	t.b.d.		For production use only – do not connect
6	GND		

Table 4-4 Programming Connector: Pinout and pin assignments



PROG-SFP is connected to the CPU pin “F12” and used for supplying the fuse programming voltage. Estimated power consumption is < 180mW.

4.2 Reset Structure

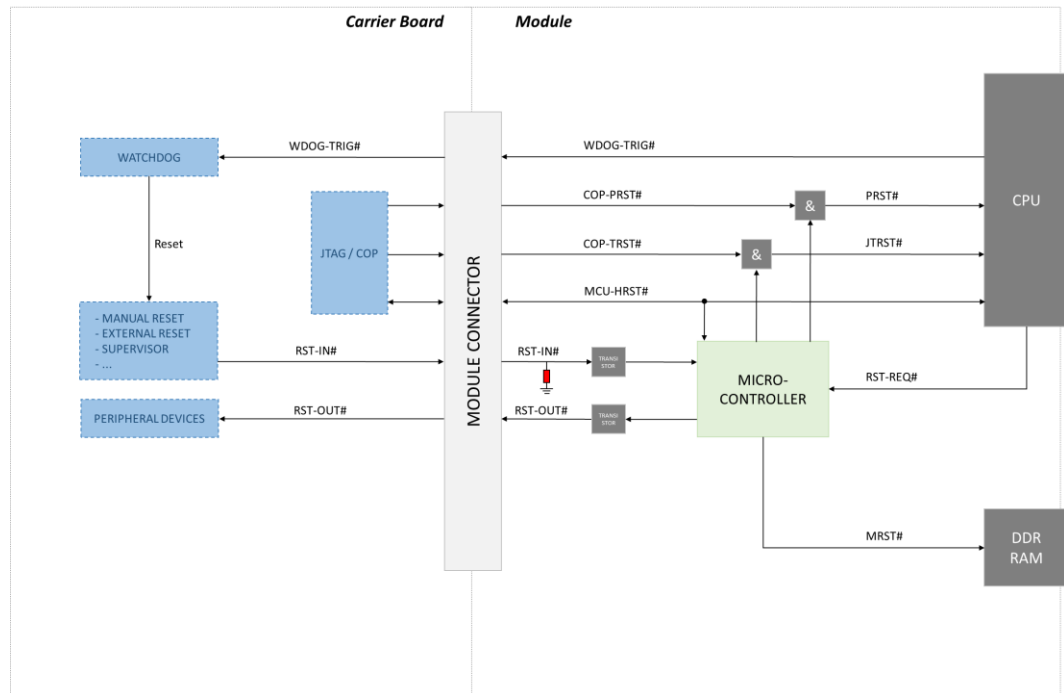


Figure 4-1 Reset structure

The reset structure of the MPX-T1042 module is shown in Figure 4-1 Reset structure. For basic operation only RST-IN# and RST-OUT# are necessary.

The RST-IN# is an input to the module. It signals that the voltage supplies on the carrier board are within their limits and no manual reset is triggered. When active (signal is low) the microcontroller unit on the module initiates the reset sequence to keep the CPU in a defined reset state. No further interaction from the carrier board is necessary. In case the module reset is active, the module triggers the RST-OUT# signal which is intended to control the reset of peripheral devices on the carrier board i.e., Ethernet PHYs, PCIe slots and devices.

MCU-HRST#, COP-PRST# and COP-TRST# are for JTAG and debugging purposes only.



The default state for RST-IN# is active. Consequently, the module is always in a reset state when the RST-IN# signal is not actively driven high by the carrier board.

The following table shows the internal connections:

CPU		Module Connector			
Ball	Signal		Pin	Signal	I/O Range Signal conditioning
-	-	←	T136	RST-IN#	Connected to base of PDTC123JQC
-	-	→	T135	RST-OUT#	Connected to collector of PDTC123JQC
AB4	GPIO1_26	←	B118	WDOG-TRIG#	1,8V PU: 4,7k
E8	HRESET#	→	B111	MCU-HRST#	1,8V PU: 1k
F13	PORESET#	←	B110	COP-PRST#	1,8V PU: 10k
E19	TRST#	→	B106	COP-TRST#	1,8V PU: 10k

Table 4-5 Reset signals: overview

4.3 Power Structure

The MPX-T1042 module is supplied by a single supply. For RTC backup buffering an additional supply from the carrier board is necessary.

The module itself does not provide any supply voltage to the carrier but it has some reference voltages that show the voltage level of the respective interface on the module. To preserve flexibility, the MPX2 standard does not specify a certain level on those pins. If necessary, the carrier board must track the reference voltages and generate a copy which can carry higher loads.

The following diagram shows the structure of the power supplies:

The following table shows the internal connections:

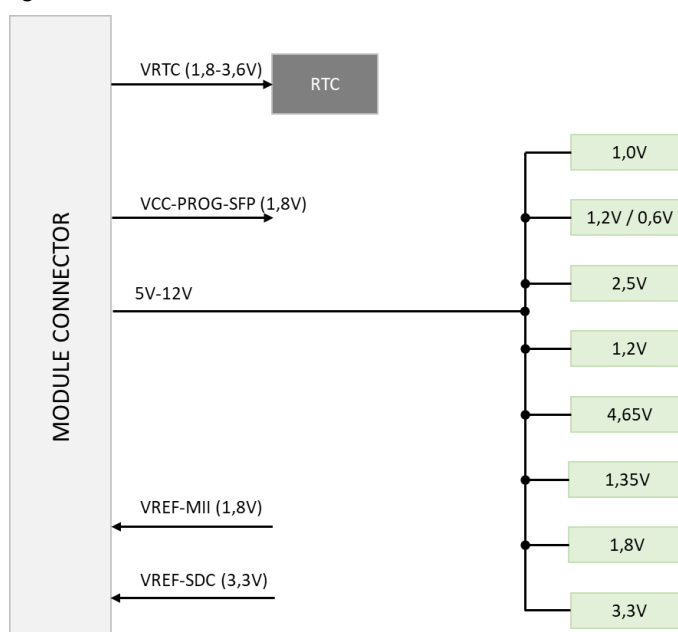


Figure 4-2 Power supplies: structure

Module Connector			
Pin	Signal	I/O Range	Signal conditioning
B80	VRTC	Typ. 1,8V-3,6V	See Figure 4-4
B81	VREF-SDC	3,3V	Maximum current to be drawn: 250mA
TK2	VCC-PROG-SFP	1,8V	
T80	VREF-MII	1,8V	Maximum current to be drawn: 250mA
T146-T154 / B148-B156	VIN	5V (-5%) up to 12V (+5%)	TVS diode protection

Table 4-6 Module connector: power pin assignments

VCC-PROG-SFP is used for fuse programming of the CPU.

The fuses are usually burnt during production test; therefore, this voltage is not mandatory. In case the customer has special requirements, a 1,8V supply with ~100mA that can be connected to the pin (and disconnected) after the module has powered up. The signal is also connected to connector ST3 (see chapter 4.1.4).



Do not permanently connect a 1.8V supply to VCC-PROG-SFP!

The power rail must be switched on and off.

The voltages which are necessary for the CPU and peripheral devices are generated from the input voltage on the module. The voltages are:

Voltage rail	Tolerance	Description
1,0V	1,0V $\pm$ 30mV	CPU core voltage
1,2V	1,2V $\pm$ 60mV	DDR4 memory voltage
0,6V	0,6V $\pm$ 25mV	DDR4 termination voltage
0,6V	0,6V $\pm$ 15mV	DDR4 reference voltage
2,5V	2,5V $\pm$ 125mV	DDR4 wordline supply voltage
1,2V	1,2V $\pm$ 20mV	Ethernet MDC2 interface voltage
4,65V	4,65V $\pm$ 100mV	Regulator bias voltage
1,35V	1,35V $\pm$ 67mV	SerDes transmitter voltage
1,0V	1,0V $\pm$ 30mV	SerDes receiver voltage
1,8V	1,8V $\pm$ 90mV	PLL, GPIO, Ethernet voltage (VREF-MII) & peripheral devices
3,3V	3,3V $\pm$ 165mV	USB, GPIO voltage (VREF-SDC) & peripheral devices

Table 4-7 Voltage rails of the module

4.4 Clock Structure

The following table shows the clocks that are available on the MPX-T1042 module connector. Onboard clocks are not displayed:

CPU			Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning	Frequency
K1	SDHC_CLK	→	B100	SDC-CLK	VREF-SDC (3,3V)	SR: 10R PU: 47k	t.b.d.
N1	SPI_CLK	→	B69	SPI-CLK	3,3V	SR: 10R	t.b.d.
W1	IIC1_SCL	→	B78	I2C1-SCL	3,3V	PU: 4,7k	400 kHz
V3	IIC2_SCL	→	B75	I2C2-SCL	3,3V	PU: 4,7k	400 kHz
E18	TCK	←	B105	JTCK	1,8V	PU: 10k	t.b.d.
AF3	EC1_TX_CLK	→	T94	MII1-TXCK	VREF-MII (1,8V)	SR: 10R	125 MHz
AD1	EC1_RX_CLK	←	T86	MII1-RXCK	VREF-MII (1,8V)	SR: 10R	125 MHz
AG3	EC1_GTX_CLK 125	←	T83	MII1-CRS	VREF-MII (1,8V)	SR: 10R	125 MHz
AE8	EC2_GTX_CLK	→	T65	MII2-TXCK	VREF-MII (1,8V)	SR: 10R	125 MHz
AH5	EC2_RX_CLK	←	T75	MII2-RXCK	VREF-MII (1,8V)		125 MHz
AC6	EC2_GTX_CLK 125	←	T77	MII2-GTXCK	VREF-MII (1,8V)		125 MHz
M4	DIU_CLK_OUT	→	B54	DIU-CLK	3,3V	SR: 10R	t.b.d.

Table 4-8 Clock: pin assignments

IDT6V49205B			Module Connector			
Pin	Signal		Pin	Signal	Signal conditioning	Frequency
30	PCleT_LR2	→	T50	SRD-CLK1+	Parallel termination: SR: 33R PD: 49R9	100 MHz / 125 MHz
29	PCleC_LR2	→	T51	SRD-CLK1-	Parallel termination: SR: 33R PD: 49R9	100 MHz / 125 MHz
32	PCleT_LR3	→	T53	SRD-CLK2+	Parallel termination: SR: 33R PD: 49R9	100 MHz / 125 MHz
31	PCleC_LR3	→	T54	SRD-CLK2-	Parallel termination: SR: 33R PD: 49R9	100 MHz / 125 MHz

Table 4-9 SerDes clock: pin assignments

4.5 Boot Sources

The MPX-T1042 module offers the option of booting from different boot devices. The term “boot device” usually refers to uboot location. It is possible to place uboot in SPI flash, for example, and load the filesystem from NAND flash.

The boot source can be selected by means of two pins:

Module Connector			
Pin	Signal	I/O Range	Signal conditioning
T134	BOOT-SEL1	1,8V	PU: 10k
T133	BOOT-SEL2	1,8V	PU: 10k

Table 4-10 Boot select pins: pin assignments

Four different boot devices are possible:

BOOT-SEL1	BOOT-SEL2	Boot Source	Description	Boot Location
HIGH	HIGH	SPI Flash	SPI Flash is accessible, CS0# is not routed to the carrier	module
HIGH	LOW	NAND Flash	SPI Flash is accessible, CS0# is not routed to the carrier	module
LOW	HIGH	SD/MMC	MMC Bus width: 8 bit SPI Flash is NOT accessible, CS0# is not routed to the carrier	carrier board
LOW	LOW	SD/MMC	MMC Bus width: 4 bit SPI Flash is accessible, CS0# is not routed to the carrier	carrier board

Table 4-11 Boot devices: overview

As shown in Table 4-11, SPI-CS0# is currently not available on the carrier board.

4.6 LEDs

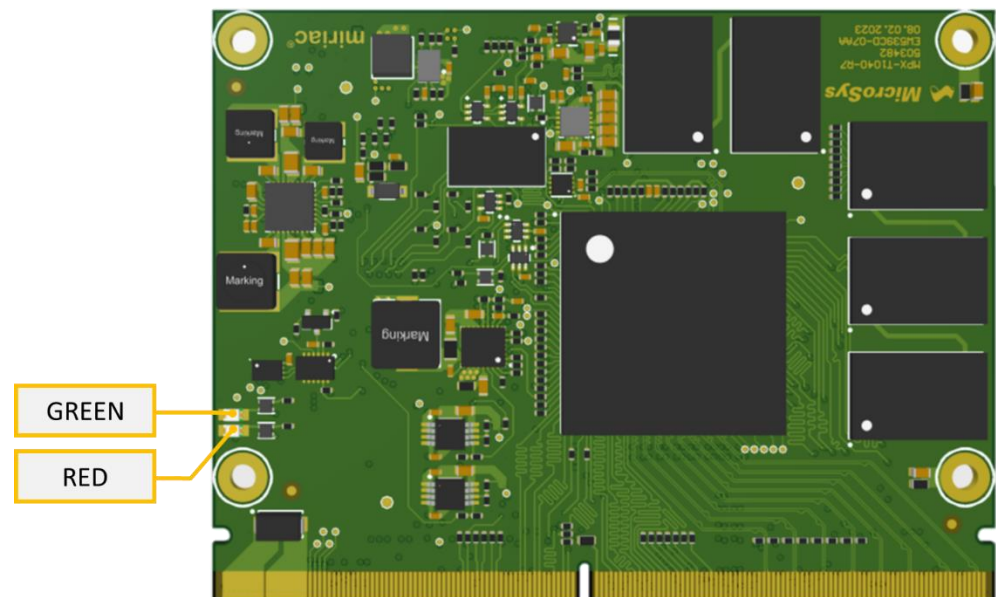


Figure 4-3 LEDs

Color	Function	
Green	LED ON:	Power-up sequence of the module is finished, power is good
	LED OFF:	Power fail
Red	LED ON:	Module reset is active
	LED BLINKING:	Overvoltage has been detected; the board needs a power cycle
	LED OFF:	Reset is inactive

Table 4-12 LED: pin description

4.7 RTC (Real-Time Clock)

The RTC is implemented with an Epson RX-8803LC chip:

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 85°C
- Deviation ~13s per month, ~156s per year
- Address see Table 4-20 I2C1: bus map

The RTC needs to be buffered on the carrier board. The following table shows the internal connection:

Module Connector			
Pin	Signal	I/O Range	Signal conditioning
B80	VRTC	Typ. 1,8V-3,6V	See Figure 4-4

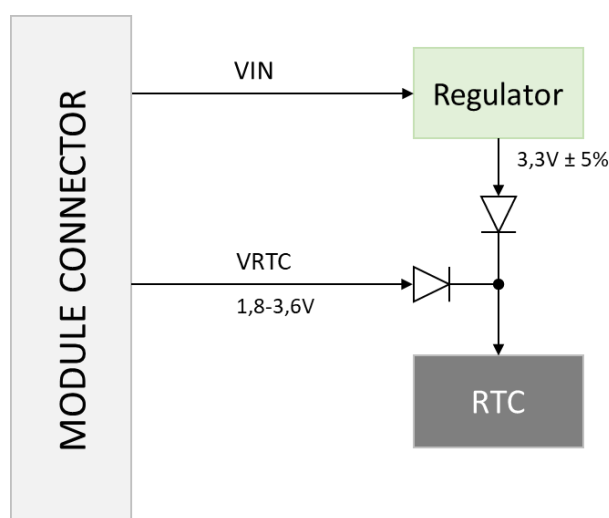


Figure 4-4 RTC: buffering

The RTC provides an interrupt which is connected to the CPU:

CPU		LM95245			
Ball	Signal	Pin	Signal	I/O Range	Signal conditioning
F7	IRQ00	← 11	INT#	1,8V	PU: 4,7k

Table 4-13 RTC: IRQs

4.8 Temperature sensor

The T1042 has an integrated temperature diode which is connected to a TMP451 temperature sensor from Texas Instruments.

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 125°C
- Address see Table 4-20 I2C1: bus map
- Local temperature monitoring (TMP451 internal temperature)
- Remote temperature monitoring (T1042 temperature diode)
- Two CPU interrupts for adjusting two temperature thresholds

	Ambient: 0°C / +70°C	Ambient: -40°C / +125°C
Local Temperature (of the sensor itself)	Max. ± 1°C	Max. ± 2°C
Remote Temperature (of the CPU internal diode)	Max. ± 1°C	Max. ± 4°C

Figure 4-5 Temperature sensor: accuracy

The temperature sensor provides two interrupts which are connected to the CPU:

CPU			TMP451			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
L4	IRQ10	←	6	ALRT#/THRM2	3,3V	PU: 4,7k
U3	IRQ11	←	4	THRM#	3,3V	PU: 4,7k

Table 4-14 Temperature sensor: IRQs

4.9 Power-up/down behavior

The module can be normally operated within 5V to 12V.

The input voltage is monitored by the microcontroller which controls the module's power-up and power-down.

Starting from power-off state requires at least 4.75V for the module to start the power-up sequence. During normal state any voltage drop of the input voltage below 4.5V causes the module to power off. In case the voltage recovers and rises above 4.75V again, the module re-starts.

The behavior is different in case any onboard created voltage is out of specification or the input voltage rises above 13.5V. If that happens, the module is switched off and the red LED is blinking. A power cycle is required to clear internally generated error flags and to re-start the module.

4.10 Interface Description

4.10.1 GPIOs

The MPX-T1042 provides GPIOs on dedicated pins. Additionally, many interfaces can be configured as GPIOs, too. For more information on the GPIO capability of each interface please refer to the corresponding chapter.



Due to dependencies between the interfaces, there can be limitations.

For more information and configuration please contact MicroSys.

The following table shows the dedicated GPIOs and their internal connections:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
E17	GPIO1_09	↔	B116	GPIO1	1,8V	
C17	GPIO1_10	↔	B117	GPIO2	1,8V	
AB4	GPIO1_26	↔	B118	GPIO3 / WDOG-TRIG#	1,8V	PU: 4,7k
B2	GPIO1_13	↔	B119	GPIO4	1,8V	PU: 4,7k
B17	GPIO1_14	↔	B120	GPIO5	1,8V	
D1	GPIO1_23	↔	B121	GPIO6	1,8V	PU: 4,7k
D4	GPIO1_24	↔	B122	GPIO7	1,8V	PU: 4,7k
D5	GPIO1_25	↔	B124	GPIO8	1,8V	PU: 4,7k

Table 4-15 GPIOs: pin assignments

With Hardware Revision 5 the number of GPIOs was expanded:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
E14	GPIO2_15	↔	B12	GPIO-E14	1,8V	
C15	GPIO2_13	↔	B15	GPIO-C15	1,8V	
C14	GPIO2_14	↔	B16	GPIO-C14	1,8V	
D18	GPIO1_11	↔	B18	GPIO-D18	1,8V	
C19	GPIO1_12	↔	B19	GPIO-C19	1,8V	

Table 4-16 GPIOs: additional GPIO pin assignments

4.10.2 JTAG/COP/Aurora

The MPX-T1042 module has a JTAG interface that is directly connected to the module connector.

The following table shows the internal connections of the JTAG interface:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
A18	TDI	←	B103	JTDI	1,8V	
C18	TDO	→	B104	JTDO	1,8V	
E18	TCK	←	B105	JTCK	1,8V	PU: 10k
B18	TMS	←	B102	JTMS	1,8V	
D19	TRST#	←	B106	COP-TRST#	1,8V	PU: 10k

Table 4-17 JTAG interface: pin assignments

Additional COP signals are also available:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
F13	PORESET#	←	B110	COP-PRST#	1,8V	PU: 10k
F18	CKSTP_OUT#	→	B109	CKSTPO#	1,8V	PU: 4,7k
E8	HRESET#	↔	B111	MCU-HRST#	1,8V	PU: 1k

Table 4-18 COP interface: pin assignments

To use the Aurora interface, the additional Aurora connector (see chapter 4.1.3) is necessary. Data will be transferred via SerDes on Lane 4 (see chapter 4.10.10).

4.10.3 I2C

The MPX-T1042 module offers a maximum of four independent I²C busses which run at up to 400kHz. While I2C1 and I2C2 have dedicated pins on the module connector, I2C4 shares its pins with DIU signals. I2C3 was introduced with Hardware Revision 5 and has now dedicated pins on the connector, too.

More information on the possible options can be found in Table 4-52 DIU: pin sharing options.



Pullups for I2C4 must be implemented on the carrier board.

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
V1	IIC1_SDA	↔	B77	I2C1_SDA	3,3V	PU: 4,7k
W1	IIC1_SCL	→	B78	I2C1_SCL	3,3V	PU: 4,7k
Y3	IIC2_SDA	↔	B74	I2C2_SDA	3,3V	PU: 4,7k
V3	IIC2_SCL	→	B75	I2C2_SCL	3,3V	PU: 4,7k
W3	IIC3_SDA	↔	B22	I2C3_SDA	3,3V	PU: 4,7k
V2	IIC3_SCL	→	B21	I2C3_SCL	3,3V	PU: 4,7k
AB3	IIC4_SDA	↔	B52	DIU-VSN	3,3V	
AA3	IIC4_SCL	→	B51	DIU-HSN	3,3V	

Table 4-19 I2C: pin assignments

I2C1 has the following layout:

Device		A6	A5	A4	A3	A2	A1	A0	R/W	7 bit
Temperature Sensor	TMP451 (slave address)	1	0	0	1	1	0	0	1/0	0x4C
	TMP451 (General Call reset address)	0	0	0	0	0	0	0	-/0	0x00
RTC	RX-8803LC	0	1	1	0	0	1	0	1/0	0x32
EEPROM	M24128	1	0	1	0	0	0	0	1/0	0x50
Clock Generator	IDT6V49205B	1	1	0	1	0	0	1	1/0	0x69

Table 4-20 I2C1: bus map

There are no devices on the I2C2 bus on the module.

4.10.4 SPI

The MPX-T1042 module provides a SPI interface with a maximum of four chip selects. Chip select CS0# can be used to select the onboard SPI flash (default: 4MB) which is also boot device. Up to 64 MB are available on request/order.

Due to limited CPU pin resources the SPI and MMC interface share pins. According to Table 4-21 there's a configuration option where the SPI flash is not accessible. In that case another boot device must be used according to chapter 4.5

There are several configuration options available which are mutually exclusive:

Configuration options	SPI-CS0#	SPI-... CS1# CS2# CS3#	SDC-D0 SDC-D1 SDC-D2 SDC-D3	SDC-D4	SDC-D5 SDC-D6 SDC-D7
	SPI Interface		SDHC Interface		
SD-CARD (1/4bit) & SPI Boot Flash & SPI on carrier board (3x Chip Select)	SPI Boot Flash	✓	✓	-	-
MMC (8bit)	-	-	✓	✓	✓

Table 4-21 SPI / SDHC implementation: options

The following table shows the internal SPI connections:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
P1	SPI-MISO	←	B72	SPI-MISO	3,3V	
P2	SPI-MOSI	→	B71	SPI-MOSI	3,3V	
N1	SPI-SCK	→	B69	SPI-CLK	3,3V	SR: 10R
M1	SPI-CS0#	→	B70	SPI-CS0#	3,3V	Signal is multiplexed
M2	SPI-CS1#	→	B93	SPI-CS1#	3,3V	
M3	SPI-CS2#	→	B92	SPI-CS2#	3,3V	
N3	SPI-CS3#	→	B91	SPI-CS3#	3,3V	

Table 4-22 SPI: pin assignments

Part of the SPI interface is multiplexed with the SDHC interface. The SPI chip select signals can also be used as GPIO. For more information see chapter 4.10.9 and Table 4-34 SDHC interface: pin sharing options.

The SPI flash has the following connections:

CPU		SPI Flash S25FL128SAGNFI00			
Ball	Signal		Pin	Signal	I/O Range
M1	SPI-CS0#	→	1	CS#	3,3V
P1	SPI-MISO	←	2	SO	3,3V
			3	W#	3,3V
			4	GND	
P2	SPI-MOSI	→	5	SI	3,3V
N1	SPI-CLK	→	6	SCK	3,3V
			7	HOLD#	3,3V
			8	VCC	3,3V

Table 4-23 SPI Flash: pin assignments

4.10.5 NAND

The MPX-T1042 module is equipped with 512MByte of NAND Flash on the IFC port of the T1042 by default. Different sizes may be available on request/order.

The following table shows the connections and signal levels for the NAND Flash:

CPU			NAND Flash S34MS04G100BHI000		
Ball	Signal		Pin	Signal	I/O Range
			G5	LOCK	1,8V
B15	IFC-RB0# (as boot device)	←	C8	RY/BY	1,8V
A15	IFC-RB1#				
D15	IFC-OE#	→	D4	RE#	1,8V
C13	IFC-CS0#	→	C6	CE#	1,8V
			D3,G4 ,H8,J6	VCC	1,8V
			C5, F7, K3, K8	GND	
F16	IFC-CLE	→	D5	CLE	1,8V
D17	IFC-AVD	→	C4	ALE	1,8V
D13	IFC-WE0#	→	C7	WE#	1,8V
F17	IFC-WP0#	→	C3	WP#	1,8V
A8	IFC-AD7	↔	H4	D0	1,8V
B8	IFC-AD6	↔	J4	D1	1,8V
A7	IFC-AD5	↔	K4	D2	1,8V
A6	IFC-AD4	↔	K5	D3	1,8V
B6	IFC-AD3	↔	K6	D4	1,8V
A5	IFC-AD2	↔	J7	D5	1,8V
B5	IFC-AD1	↔	K7	D6	1,8V
A4	IFC-AD0	↔	J8	D7	1,8V
			G3	n.c.	
			G8	n.c.	

Table 4-24 NAND Flash: pin assignments

4.10.6 nvSRAM

The MPX-T1042 module is equipped with nvSRAM on the IFC port of the T1042.

- Connected to chip select 1
- 16 bit data bus
- Address support up to 8 Mbit (default: 1 Mbit)
- Byte access

4.10.7 USB

The MPX-T1042 has a maximum of two USB2.0 ports which can be configured as host or device.

All ports support high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations.

The following table shows the internal connections:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
E4	USB1_VBUSCLMP	←	B133	USB1-VBUS	5V	See Figure 4-6
F4	USB1_UID	←	B130	USB1-UID	1,8V	
F1	USB1_UDP	↔	T130	USB1-D+		
F2	USB1_UDM	↔	T131	USB1-D-		

Table 4-25 USB port 1: pin assignments

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
J4	USB2_VBUSCLMP	←	B128	USB2-VBUS	5V	See Figure 4-6
H4	USB2_UID	←	B125	USB2-UID	1,8V	
H1	USB2_UDP	↔	T127	USB2-D+		
H2	USB2_UDM	↔	T128	USB2-D-		

Table 4-26 USB port 2: pin assignments

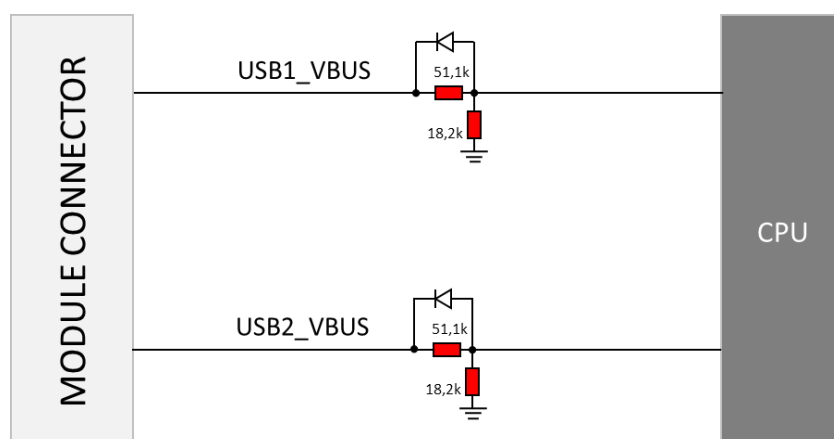


Figure 4-6 USBx-VBUS wiring diagram

Moreover, the module provides control signals on dedicated pins. Each port can be individually enabled and has an overcurrent signal on its own.

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
F6	USB1_DRVVBUS	→	B132	USB1-EN	3,3V	
F5	USB1_PWRFAULT	←	B131	USB1-OC	3,3V	PD: 47k
J5	USB2_DRVVBUS	→	B127	USB2-EN	3,3V	
H5	USB2_PWRFAULT	←	B126	USB2-OC	3,3V	PD: 47k

Table 4-27 USB power control signals: pin assignments



USBx_PWRFAULT signals are high-active signals.
A logic high level signals the port is in an overcurrent situation.

4.10.8 UART

The MPX-T1042 module provides a maximum of four UARTs which can be configured in two ways:

- Two UARTs w/ hardware handshake signals -or-
- Four UARTs w/o hardware handshake signals (RX/TX only)

Configuration is done by software via RCW.

The following table shows the internal connections for two UARTs:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AA1	UART1_SIN	←	B37	UART1-RXD	3,3V	
AA2	UART1_SOUT	→	B38	UART1-TXD	3,3V	
Y2	UART1_CTS#	←	B39	UART1-CTS#	3,3V	PU: 4,7k
Y1	UART1_RTS#	→	B40	UART1-RTS#	3,3V	PU: 4,7k
W4	UART2_SIN	←	B32	UART2-RXD	3,3V	
AA4	UART2_SOUT	→	B33	UART2-TXD	3,3V	
Y4	UART2_CTS#	←	B34	UART2-CTS#	3,3V	PU: 4,7k
V4	UART2_RTS#	→	B35	UART2-RTS#	3,3V	PU: 4,7k

Table 4-28 UART w/ hardware handshake: pin assignments

The following table shows the internal connections for four UARTs:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AA1	UART1_SIN	←	B37	UART1-RXD	3,3V	
AA2	UART1_SOUT	→	B38	UART1-TXD	3,3V	
Y2	UART3_SIN	←	B39	UART3-RXD	3,3V	PU: 4,7k
Y1	UART3_SOUT	→	B40	UART3-TXD	3,3V	PU: 4,7k
W4	UART2_SIN	←	B32	UART2-RXD	3,3V	
AA4	UART2_SOUT	→	B33	UART2-TXD	3,3V	
Y4	UART4_SIN	←	B34	UART4-RXD	3,3V	PU: 4,7k
V4	UART4_SOUT	→	B35	UART4-TXD	3,3V	PU: 4,7k

Table 4-29 UART w/o hardware handshake: pin assignments



UART1 is the serial debug console of the MPX-T1042 module but can be configured as GPIOs as well.

The following tables list the pin sharing options for UART1 and UART2:

CPU pin sharing			Module Connector	
Ball	Primary function	Secondary function	Pin	Description
AA1	UART1_SIN	GPIO1_17	B37	configurable as GPIO
AA2	UART1_SOUT	GPIO1_15	B38	configurable as GPIO
Y2	UART1_CTS#	GPIO1_21	B39	configurable as GPIO
Y1	UART1_RTS#	GPIO1_19	B40	configurable as GPIO

Table 4-30 UART1 interface: pin sharing options

CPU pin sharing			Module Connector	
Ball	Primary function	Secondary function	Pin	Description
W4	UART2_SIN	GPIO1_18	B32	configurable as GPIO
AA4	UART2_SOUT	GPIO1_16	B33	configurable as GPIO
Y4	UART2_CTS#	GPIO1_22	B34	configurable as GPIO
V4	UART2_RTS#	GPIO1_20	B35	configurable as GPIO

Table 4-31 UART2 interface: pin sharing options

4.10.9 eSDHC

The MPX-T1042 module supports SD/SDIO cards (1/4 bit) and eMMC devices (1/4/8 bit). DDR modes are not supported.



The eMMC interface (8 bit) and the SPI interface share pins, thus 8-bit support and SPI are mutually exclusive.

The following table shows the internal connections:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
K3	SDHC_CMD	↔	B99	SDC-CMD	VREF-SDC (3,3V)	PU: 47k
K1	SDHC_CLK	→	B100	SDC-CLK	VREF-SDC (3,3V)	SR: 10R PU: 47k
L2	SDHC_DAT0	↔	B98	SDC-D0	VREF-SDC (3,3V)	PU: 47k
K4	SDHC_DAT1	↔	B97	SDC-D1	VREF-SDC (3,3V)	PU: 47k
L3	SDHC_DAT2	↔	B96	SDC-D2	VREF-SDC (3,3V)	PU: 47k
L1	SDHC_DAT3	↔	B95	SDC-D3	VREF-SDC (3,3V)	PU: 47k
M1	SDHC_DAT4	↔	B94	SDC-D4	VREF-SDC (3,3V)	
M2	SDHC_DAT5	↔	B93	SDC-D5	VREF-SDC (3,3V)	
M3	SDHC_DAT6	↔	B92	SDC-D6	VREF-SDC (3,3V)	
N3	SDHC_DAT7	↔	B91	SDC-D7	VREF-SDC (3,3V)	

Table 4-32 SDHC interface: pin assignments

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
L5	SDHC_CD#	←	B90	SDC-CD#	VREF-SDC (3,3V)	PU: 47k
M5	SDHC_WP	←	B89	SDC-WP	VREF-SDC (3,3V)	PD: 47k
		→	B81	VREF-SDC	3,3V	Up to 250mA

Table 4-33 SDHC control interface: pin assignments

The “VREF-SDC” is a reference voltage which indicates the level of the supply voltage of the SDHC interface of the T1042. This voltage can vary within the MPX module family but is fixed to 3,3V for the MPX-T1042 module.



The “VREF-SDC” voltage may be loaded up to 250mA. In case more current needs to be drawn, the voltage must be tracked on the carrier board.

The SDHC interface can alternatively be configured as GPIOs.

The following table lists the possible functions:

CPU pin sharing				Module Connector	
Ball	Primary function	Secondary function	Tertiary function	Pin	Description
K3	SDHC_CMD	GPIO2_04		B99	
K1	SDHC_CLK	GPIO2_09		B100	
L2	SDHC_DAT0	GPIO2_05		B98	
K4	SDHC_DAT1	GPIO2_06		B97	
L3	SDHC_DAT2	GPIO2_07		B96	
L1	SDHC_DAT3	GPIO2_08		B95	
M1	SPI-CS0#	GPIO2_00		B70	Pin multiplexing via system controller
			SDHC_DAT4	B94	
M2	SPI-CS1#	GPIO2_01	SDHC_DAT5	B93	
M3	SPI-CS2#	GPIO2_02	SDHC_DAT6	B92	
N3	SPI-CS3#	GPIO2_03	SDHC_DAT7	B91	
L5	SDHC_CD#	GPIO4_24		B90	SDHC card detect
M5	SDHC_WP	GPIO4_25		B89	SDHC write protect

Table 4-34 SDHC interface: pin sharing options

4.10.10 SerDes

The MPX-T1042 module offers eight SerDes lanes. These lanes can be configured according to the T1042 reference manual provided by manufacturer NXP. More information on the MAC capabilities can be found in chapter 4.10.11.



SerDes mapping is configurable via RCW.

For more information on possible configurations please contact MicroSys.

The following table shows a mapping example in a configuration setup that is used on the SBC-T1042 starterkit:

■ SerDes 1: 0x86

	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
PCIe	✓				✓	✓		
SGMII		✓	✓	✓			✓	
SATA								✓

Table 4-35 SerDes interface: mapping example

The eight SerDes lanes can support different protocols. Some of the protocols are available on specific lanes only. The following table shows the distribution across those lanes. Not all combinations are valid:

Lane on module connector:	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
		MAC3	MAC1	MAC2			MAC4	MAC5
PCIe x1	✓				✓	✓	✓	
PCIe x2	✓ (Lane 0/1)				✓ (Lane 4/5)			
PCIe x4	✓ (Lane 0/1/2/3)				✓ (Lane 4/5/6/7)			
SGMII (1 Gbps)		✓	✓	✓			✓	✓
SGMII (2,5 Gbps)			✓	✓				
SATA							✓	✓
Aurora					✓			

Table 4-36 MAC distribution

The MPX-T1042 module also provides two clock pairs which are displayed in Table 4-9. The frequency on those pins depends on the configuration of the SerDes lanes as different interfaces require clocks at either 100MHz or 125MHz.

The following table shows the internal connections of the SerDes lanes:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AD10	SD-TX0	→	T47	SRD-TX0+		AC-coupling: 100nF
AE10	SD-TX0#	→	T48	SRD-TX0-		AC-coupling: 100nF
AH10	SD-RX0	←	T44	SRD-RX0+		
AG10	SD-RX0#	←	T45	SRD-RX0-		
AD11	SD-TX1	→	T41	SRD-TX1+		AC-coupling: 100nF
AE11	SD-TX1#	→	T42	SRD-TX1-		AC-coupling: 100nF
AH11	SD-RX1	←	T38	SRD-RX1+		
AG11	SD-RX1#	←	T39	SRD-RX1-		
AD13	SD-TX2	→	T35	SRD-TX2+		AC-coupling: 100nF
AE13	SD-TX2#	→	T36	SRD-TX2-		AC-coupling: 100nF
AH13	SD-RX2	←	T32	SRD-RX2+		
AG13	SD-RX2#	←	T33	SRD-RX2-		
AD14	SD-TX3	→	T29	SRD-TX3+		AC-coupling: 100nF
AE14	SD-TX3#	→	T30	SRD-TX3-		AC-coupling: 100nF
AH14	SD-RX3	←	T26	SRD-RX3+		
AG14	SD-RX3#	←	T27	SRD-RX3-		
AD16	SD-TX4	→	T23	SRD-TX4+		AC-coupling: 100nF
AE16	SD-TX4#	→	T24	SRD-TX4-		AC-coupling: 100nF
AH16	SD-RX4	←	T20	SRD-RX4+		
AG16	SD-RX4#	←	T21	SRD-RX4-		
AD17	SD-TX5	→	T17	SRD-TX5+		AC-coupling: 100nF
AE17	SD-TX5#	→	T18	SRD-TX5-		AC-coupling: 100nF
AH17	SD-RX5	←	T14	SRD-RX5+		
AG17	SD-RX5#	←	T15	SRD-RX5-		
AD19	SD-TX6	→	T11	SRD-TX6+		AC-coupling: 100nF
AE19	SD-TX6#	→	T12	SRD-TX6-		AC-coupling: 100nF
AH19	SD-RX6	←	T8	SRD-RX6+		
AG19	SD-RX6#	←	T9	SRD-RX6-		
AD20	SD-TX7	→	T5	SRD-TX7+		AC-coupling: 100nF
AE20	SD-TX7#	→	T6	SRD-TX7-		AC-coupling: 100nF
AH20	SD-RX7	←	T2	SRD-RX7+		
AG20	SD-RX7#	←	T3	SRD-RX7-		

Table 4-37 SerDes interface: pin assignments

4.10.11 RGMII / MII

The MPX-T1042 module provides two RGMII ports or, alternatively, one MII port.

The Frame Manager of the T1042 supports five MACs with different protocols as summarized in the following table made available by NXP:

MAC	MI (10 / 100)	RGMII (1 Gbps)	SGMII (1 Gbps)	SGMII (2,5 Gbps)
1	-	-	✓	✓
2	✓	✓	✓	✓
3	-	-	✓	-
4	✓	✓	✓	-
5	-	✓	✓	-

Table 4-38 MAC capabilities: (RG)MII, SGMII

Ethernet controller 1 (RGMII1) can use MAC2/MAC4, whereas MAC5 can be on the Ethernet controller 2 (RGMII2) interface.

The following table shows the internal connections of RGMII1:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AD1	EC1_RX_CLK	←	T86	MII1-RXCK	VREF-MII (1,8V)	
AG2	EC1_RX_CTL	←	T95	MII1-RXCTL	VREF-MII (1,8V)	
AF2	EC1_RXD0	←	T88	MII1-RXD0	VREF-MII (1,8V)	
AF1	EC1_RXD1	←	T89	MII1-RXD1	VREF-MII (1,8V)	
AE1	EC1_RXD2	←	T91	MII1-RXD2	VREF-MII (1,8V)	
AD2	EC1_RXD3	←	T92	MII1-RXD3	VREF-MII (1,8V)	
AF3	EC1_GTX_CLK	→	T94	MII1-TXCK	VREF-MII (1,8V)	SR: 10R
AE3	EC1_TXD0	→	T97	MII1-TXD0	VREF-MII (1,8V)	SR: 10R
AE4	EC1_TXD1	→	T98	MII1-TXD1	VREF-MII (1,8V)	SR: 10R
AD3	EC1_TXD2	→	T100	MII1-TXD2	VREF-MII (1,8V)	SR: 10R
AC3	EC1_TXD3	→	T101	MII1-TXD3	VREF-MII (1,8V)	SR: 10R
AF4	EC1_TX_CTL	→	T103	MII1-TXCTL	VREF-MII (1,8V)	SR: 10R
AH4	EMI1_MDIO	↔	B87	MII1-MDIO	VREF-MII (1,8V)	PU: 10k

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AH3	EMI1_MDC	→	B86	MII1-MDC	VREF-MII (1,8V)	PU: 10k SR: 10R
AG3	EC1_GTX_CLK125	←	T83	MII1-CLK125	VREF-MII (1,8V)	SR: 10R

Table 4-39 RGMII1: pin assignments

The next table shows the internal connections of RGMII2:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AH5	EC2_RX_CLK	←	T75	MII2-RXCK	VREF-MII (1,8V)	
AG8	EC2_RX_CTL	←	T66	MII2-RXCTL	VREF-MII (1,8V)	
AH8	EC2_RXD0	←	T68	MII2-RXD0	VREF-MII (1,8V)	
AG7	EC2_RXD1	←	T69	MII2-RXD1	VREF-MII (1,8V)	
AH7	EC2_RXD2	←	T71	MII2-RXD2	VREF-MII (1,8V)	
AH6	EC2_RXD3	←	T72	MII2-RXD3	VREF-MII (1,8V)	
AE8	EC2_GTX_CLK	→	T65	MII2-TXCK	VREF-MII (1,8V)	SR: 10R
AE7	EC2_TXD0	→	T59	MII2-TXD0	VREF-MII (1,8V)	SR: 10R
AF7	EC2_TXD1	→	T60	MII2-TXD1	VREF-MII (1,8V)	SR: 10R
AF6	EC2_TXD2	→	T62	MII2-TXD2	VREF-MII (1,8V)	SR: 10R
AG5	EC2_TXD3	→	T63	MII2-TXD3	VREF-MII (1,8V)	SR: 10R
AF8	EC2_TX_CTL	→	T56	MII2-TXCTL	VREF-MII (1,8V)	SR: 10R
AC6	EC2_GTX_CLK125	←	T77	MII2-CLK125	VREF-MII (1,8V)	

Table 4-40 RGMII2: pin assignments

The following table shows the internal connections of the Ethernet controller configured as MII interface:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AD1	EC1_RX_CLK	←	T86	MII1-RXCK	VREF-MII (1,8V)	
AG2	EC1_RX_DV	←	T95	MII1-RXDV	VREF-MII (1,8V)	
AC2	EC1_RX_ER	←	T85	MII1-RXER	VREF-MII (1,8V)	
AF2	EC1_RXD0	←	T88	MII1-RXD0	VREF-MII (1,8V)	
AF1	EC1_RXD1	←	T89	MII1-RXD1	VREF-MII (1,8V)	
AE1	EC1_RXD2	←	T91	MII1-RXD2	VREF-MII (1,8V)	
AD2	EC1_RXD3	←	T92	MII1-RXD3	VREF-MII (1,8V)	
AF3	EC1_TX_CLK	→	T94	MII1-TXCK	VREF-MII (1,8V)	SR: 10R
AF4	EC1_TX_EN	→	T103	MII1-TXEN	VREF-MII (1,8V)	SR: 10R
AC4	EC1_TX_ER	→	T104	MII1-TXER	VREF-MII (1,8V)	SR: 10R
AE3	EC1_TXD0	→	T97	MII1-TXD0	VREF-MII (1,8V)	SR: 10R
AE4	EC1_TXD1	→	T98	MII1-TXD1	VREF-MII (1,8V)	SR: 10R
AD3	EC1_TXD2	→	T100	MII1-TXD2	VREF-MII (1,8V)	SR: 10R
AC3	EC1_TXD3	→	T101	MII1-TXD3	VREF-MII (1,8V)	SR: 10R
AH4	EMI1_MDIO	↔	B87	MII1-MDIO	VREF-MII (1,8V)	PU: 10k
AH3	EMI1_MDC	→	B86	MII1-MDC	VREF-MII (1,8V)	PU: 10k SR: 10R
AG3	EC1_CRS	←	T83	MII1-CRS	VREF-MII (1,8V)	SR: 10R
AC1	EC1_COL	←	T82	MII1-COL	VREF-MII (1,8V)	

Table 4-41 MII: pin assignments

The RGMII interfaces can also be configured and used as GPIOs:

CPU pin sharing			Module Connector	
Ball	Primary function	Secondary function	Pin	Description
AD1	EC1_RX_CLK	GPIO3_23	T86	configurable as GPIO
AG2	EC1_RX_CTL	GPIO3_22	T95	configurable as GPIO
AF2	EC1_RXD0	GPIO3_21	T88	configurable as GPIO
AF1	EC1_RXD1	GPIO3_20	T89	configurable as GPIO
AE1	EC1_RXD2	GPIO3_19	T91	configurable as GPIO
AD2	EC1_RXD3	GPIO3_18	T92	configurable as GPIO
AF3	EC1_GTX_CLK	GPIO3_16	T94	configurable as GPIO
AE3	EC1_TXD0	GPIO3_14	T97	configurable as GPIO
AE4	EC1_TXD1	GPIO3_13	T98	configurable as GPIO
AD3	EC1_TXD2	GPIO3_12	T100	configurable as GPIO
AC3	EC1_TXD3	GPIO3_11	T101	configurable as GPIO
AF4	EC1_TX_CTL	GPIO3_15	T103	configurable as GPIO

Table 4-42 RGMII1: pin sharing options

CPU pin sharing			Module Connector	
Ball	Primary function	Secondary function	Pin	Description
AH5	EC2_RX_CLK	GPIO4_31	T75	configurable as GPIO
AG8	EC2_RX_CTL	GPIO4_30	T66	configurable as GPIO
AH8	EC2_RXD0	GPIO3_31	T68	configurable as GPIO
AG7	EC2_RXD1	GPIO3_30	T69	configurable as GPIO
AH7	EC2_RXD2	GPIO3_29	T71	configurable as GPIO
AH6	EC2_RXD3	GPIO3_28	T72	configurable as GPIO
AE8	EC2_GTX_CLK	GPIO4_28	T65	configurable as GPIO
AE7	EC2_TXD0	GPIO3_27	T59	configurable as GPIO
AF7	EC2_TXD1	GPIO3_26	T60	configurable as GPIO
AF6	EC2_TXD2	GPIO3_25	T62	configurable as GPIO
AG5	EC2_TXD3	GPIO3_24	T63	configurable as GPIO
AF8	EC2_TX_CTL	GPIO4_27	T56	configurable as GPIO
AC6	EC2_GTX_CLK125	GPIO4_29	T83	configurable as GPIO

Table 4-43 RGMII2: pin sharing options

4.10.12 IEEE1588

The MPX-T1042 provides IEEE1588 hardware timestamping.

The following table shows the internal connections:

CPU		Module Connector			
Ball	Signal		Pin	Signal	I/O Range Signal conditioning
AD7	TSEC_1588_CLK_OUT	→	B42	1588-CLKO	VREF-MII (1,8V)
AC8	TSEC_1588_CLK_IN	←	B43	1588-CLKI	VREF-MII (1,8V) PD: 4,7k
AD8	TSEC_1588_PULSE_OUT2	→	B44	1588-PLSO2	VREF-MII (1,8V)
AE6	TSEC_1588_PULSE_OUT1	→	B45	1588-PLSO1	VREF-MII (1,8V)
AE5	TSEC_1588_TRIG_IN2	←	B46	1588-TRGI2	VREF-MII (1,8V) PD: 4,7k
AB6	TSEC_1588_TRIG_IN1	←	B47	1588-TRGI1	VREF-MII (1,8V) PD: 4,7k
AC7	TSEC_1588_ALARM_OUT2	→	B48	1588-ALRO2	VREF-MII (1,8V)
AF5	TSEC_1588_ALARM_OUT1	→	B49	1588-ALRO1	VREF-MII (1,8V)

Table 4-44 IEEE1588: pin assignments

The interface can alternatively be configured as GPIO:

CPU pin sharing			Module Connector	
Ball	Primary function	Secondary function	Pin	Description
AD7	TSEC_1588_CLK_OUT	GPIO3_05	B42	
AC8	TSEC_1588_CLK_IN	GPIO3_00	B43	
AD8	TSEC_1588_PULSE_OUT2	GPIO3_07	B44	
AE6	TSEC_1588_PULSE_OUT1	GPIO3_06	B45	
AE5	TSEC_1588_TRIG_IN2	GPIO3_02	B46	
AB6	TSEC_1588_TRIG_IN1	GPIO3_01	B47	
AC7	TSEC_1588_ALARM_OUT2	GPIO3_04	B48	
AF5	TSEC_1588_ALARM_OUT1	GPIO3_03	B49	

Table 4-45 IEEE1588: pin sharing

4.10.13 Quicc Engine

The QUICC Engine block consists of several communication peripheral controllers. It supports various protocols.

The QUICC Engine block of the T1042 CPU has the following features:

- 32-bit RISC controller
- Serial DMA channel for receive and transmit on all serial channels
- Two TDM interfaces with T1/E1/J1 serial interfaces
- Two UCC controller (HDLC/Transparent)

The following signals are available on the module connector:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
U4	TDMB_RXD	←	B3	TDMB-RXD	3,3V	
T4	TDMB_TXD	→	B4	TDMB-TXD	3,3V	
R3	TDMB_TSYNC	←	B5	TDMB-TSYNC	3,3V	
T3	TDMB_RSYNC	←	B6	TDMB-RSYNC	3,3V	
R4	TDMB_RQ	→	B7	TDMB-RQ	3,3V	
U2	TDMA_RXD	←	B9	TDMA-RXD	3,3V	
T1	TDMA_TXD	→	B10	TDMA-TXD	3,3V	
R1	TDMA_TSYNC	←	B11	TDMA-TSYNC	3,3V	
U1	TDMA_RSYNC	←	B12	TDMA-RSYNC	3,3V	
R2	TDMA_RQ	→	B13	TDMA-RQ	3,3V	
P4	CLK9	←	B18	QE-CLK1	3,3V	
P3	CLK10	←	B19	QE-CLK2	3,3V	
N4	CLK11	←	B21	QE-CLK3	3,3V	
M4	CLK12	←	B22	QE-CLK4	3,3V	SR: 33R

Table 4-46 Quicc Engine: pin assignments

The Quicc Engine is not the primary interface available on the CPU pins. They are shared with the display unit. Furthermore, the pins can be configured as GPIOs as well. For pin sharing options see Table 4-52 DIU: pin sharing options.

4.10.14 TDM

The Time Division Multiplexing Interface (TDM) of the T1042 offers independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs. Up to 128 time slots are possible. More information can be obtained from NXP's reference manual.

The following table presents an overview of the TDM signals:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
U5	TDM_TFS	↔	B26	TDM-TFS	3,3V	SR: 49R9
R5	TDM_TCK	↔	B30	TDM-TCK	3,3V	SR: 49R9
P5	TDM_TXD	→	B27	TDM-TXD	3,3V	SR: 49R9
AA5	TDM_RFS	↔	B24	TDM-RFS	3,3V	SR: 49R9
Y5	TDM_RCK	↔	B29	TDM-RCK	3,3V	SR: 49R9
V5	TDM_RXD	←	B25	TDM-RXD	3,3V	SR: 49R9

Table 4-47 TDM: pin assignments

The TDM interface is shared with DMA control signals and can alternatively be configured as GPIO:

CPU pin sharing				Module Connector	
Ball	Primary function	Secondary function	Tertiary function	Pin	Description
U5	TDM_TFS	DMA1_DACK0#	GPIO4_05	B26	
R5	TDM_TCK	DMA1_DDONE0#	GPIO4_06	B30	
P5	TDM_TXD	DMA1_DREQ0#	GPIO4_04	B27	
AA5	TDM_RFS	DMA2_DACK0#	GPIO4_08	B24	
Y5	TDM_RCK	DMA2_DDONE0#	GPIO4_09	B29	
V5	TDM_RXD	DMA2_DREQ0#	GPIO4_07	B25	

Table 4-48 TDM: pin sharing options

4.10.15 DMA

The MPX-T1042 also provides DMA control signals for eight high-speed DMA channels.

The following table presents an overview of the DMA signals:

CPU		Module Connector				
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
U5	DMA1_DACK0#	↔	B26	TDM-TFS	3,3V	SR: 49R9
R5	DMA1_DDONE0#	↔	B30	TDM-TCK	3,3V	SR: 49R9
P5	DMA1_DREQ0#	→	B27	TDM-TXD	3,3V	SR: 49R9
AA5	DMA2_DACK0#	↔	B24	TDM-RFS	3,3V	SR: 49R9
Y5	DMA2_DDONE0#	↔	B29	TDM-RCK	3,3V	SR: 49R9
V5	DMA2_DREQ0#	←	B25	TDM-RXD	3,3V	SR: 49R9

Table 4-49 DMA: pin assignments

The DMA interface is shared with the TDM interface and can alternatively be configured as GPIO. An overview can be found in Table 4-48 TDM: pin sharing options.

4.10.16 Display Interface Unit (DIU)

The display controller of the T1042 can control a single display connected via parallel TTL. Detailed information can be found in NXP's T1042 reference manual. The key features are:

- Single plane: resolution up to 1280x1024
- Three planes: resolution up to 1024x768
- Color depth: up to 24 bpp
- RGB and 256 level gray scale supported

The display controller is internally connected as follows:

CPU		Module Connector			
Ball	Signal		Pin	Signal	I/O Range Signal conditioning
U2	DIU_D0	→	B67	DIU-D0	3,3V
U1	DIU_D1	→	B66	DIU-D1	3,3V
T1	DIU_D2	→	B65	DIU-D2	3,3V
R1	DIU_D3	→	B64	DIU-D3	3,3V
R2	DIU_D4	→	B63	DIU-D4	3,3V
U4	DIU_D5	→	B62	DIU-D5	3,3V
T3	DIU_D6	→	B61	DIU-D6	3,3V
T4	DIU_D7	→	B60	DIU-D7	3,3V
R3	DIU_D8	→	B59	DIU-D8	3,3V
R4	DIU_D9	→	B58	DIU-D9	3,3V
P4	DIU_D10	→	B57	DIU-D10	3,3V
P3	DIU_D11	→	B56	DIU-D11	3,3V
M4	DIU_CLK_OUT	→	B54	DIU-CLK	3,3V SR: 10R
N4	DIU_DE	→	B53	DIU-DE	3,3V
AB3	DIU-VSYNC	→	B52	DIU-VSYNC	3,3V
AA3	DIU-HSYNC	→	B51	DIU-HSYNC	3,3V

Table 4-50 DIU: pin assignments

The following table describes the pixel data mapping according to NXP:

Data bus	P0a	P0b	P1a	P1b	Pxa	Pxb
D11	Green0[3]	Red0[7]	Green1[3]	Red1[7]	GreenX[3]	RedX[7]
D10	Green0[2]	Red0[6]	Green1[2]	Red1[6]	GreenX[2]	RedX[6]
D9	Green0[1]	Red0[5]	Green1[1]	Red1[5]	GreenX[1]	RedX[5]
D8	Green0[0]	Red0[4]	Green1[0]	Red1[4]	GreenX[0]	RedX[4]
D7	Blue0[7]	Red0[3]	Blue1[7]	Red1[3]	BlueX[7]	RedX[3]
D6	Blue0[6]	Red0[2]	Blue1[6]	Red1[2]	BlueX[6]	RedX[2]
D5	Blue0[5]	Red0[1]	Blue1[5]	Red1[1]	BlueX[5]	RedX[1]
D4	Blue0[4]	Red0[0]	Blue1[4]	Red1[0]	BlueX[4]	RedX[0]
D3	Blue0[3]	Green0[7]	Blue1[3]	Green1[7]	BlueX[3]	GreenX[7]
D2	Blue0[2]	Green0[6]	Blue1[2]	Green1[6]	BlueX[2]	GreenX[6]
D1	Blue0[1]	Green0[5]	Blue1[1]	Green1[5]	BlueX[1]	GreenX[5]
D0	Blue0[0]	Green0[4]	Blue1[0]	Green1[4]	BlueX[0]	GreenX[4]

Table 4-51 DIU: pixel data mapping

The DIU interface can also be configured as GPIO or Quicc Engine interface. Additionally, another I²C port is available on two of the pins. The pin sharing options are summarized in the following table:

CPU pin sharing				Module Connector	
Ball	Primary function	Secondary function	Tertiary function	Pin	Description
U2	DIU_D0	TDMA_RXD	GPIO4_10	B67	
U1	DIU_D1	TDMA_RSYNC	GPIO4_11	B66	
T1	DIU_D2	TDMA_TXD	GPIO4_12	B65	
R1	DIU_D3	TDMA_TSYNC	GPIO4_13	B64	
R2	DIU_D4	TDMA_RQ	GPIO4_14	B63	
U4	DIU_D5	TDMA_RXD	GPIO4_17	B62	
T3	DIU_D6	TDMA_RSYNC	GPIO4_18	B61	
T4	DIU_D7	TDMA_TXD	GPIO4_19	B60	
R3	DIU_D8	TDMA_TSYNC	GPIO4_20	B59	
R4	DIU_D9	TDMA_RQ	GPIO4_21	B58	
P4	DIU_D10	CLK09	GPIO4_15	B57	
P3	DIU_D11	CLK10	GPIO4_22	B56	
M4	DIU_CLK_O UT	CLK12	GPIO4_23	B54	
N4	DIU_DE	CLK11	GPIO4_16	B53	
AB3	DIU-VSYNC	IIC4_SDA	GPIO4_03	B52	
AA3	DIU-HSYNC	IIC4_SCL	GPIO4_02	B51	

Table 4-52 DIU: pin sharing options

5 Mechanical Description

5.1 Edge Finger

The MPX-T1040 module is connected with the carrier board via a 314 pin connector with 0,5mm pitch. It accepts edge cards with a thickness of 1,2mm.

The pin layout is asymmetric, so the pins are unequally distributed among top and bottom side edge fingers.



Hardware Revision 5 introduced 4 additional pins. This is possible by using a 314 pin connector instead of a 310pin connector as in Hardware Revision 1 to 4.

Those four additional signals are in the former key area where the 314pin connector has physical pins instead.

Those four additional pins named "TK1, TK2, BK1, BK2" are inserted between T9/T10 on top side and B9/B10 on bottom side.

The pin numbering has not been shifted!

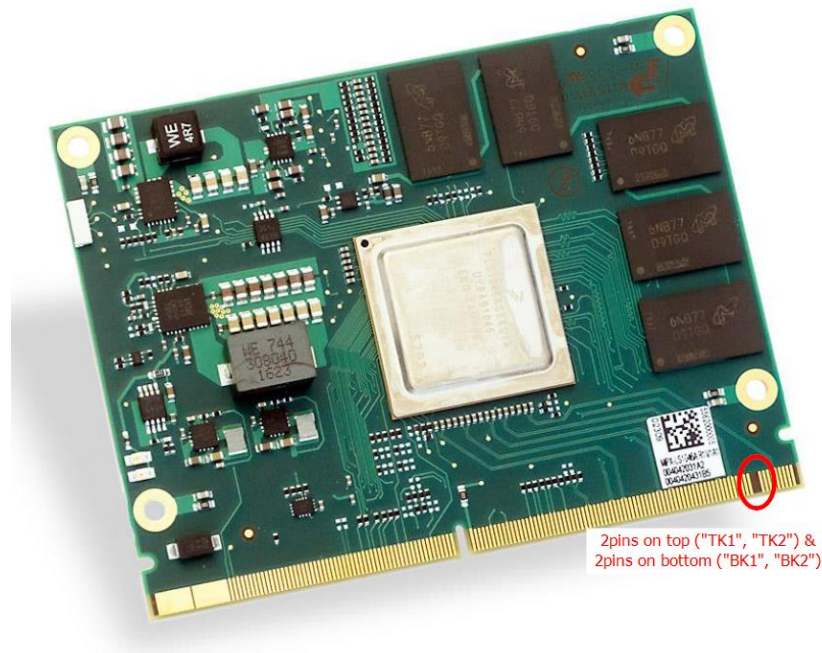


Figure 5-1 Additional Key Pins (shown on a MPX-LS1046A: identical for MPX-T1040)

There are 314 pins defined. Be careful, there are more pins on the bottom side than on the top side since the pin layout is asymmetric:

Bottom Side	158 pins	Pin labels: "B1", ... „B9“, „BK1“, „BK2“, „B10“ ... "B155", "B156"
Top Side	156 pins	Pin labels: "T1", ... "T9", „TK1“, „TK2“, "T10", ... "T153", "T154"

Table 5-1 Connector pin naming scheme

Figure 5-2 Connector orientation

The module connector is usually used for MXM3 graphic cards commonly found in notebooks. Other than that, MicroSys changed the pin layout so all the physically available 314 pins can be used.

Basically, there are more connectors on the market that can be used if there are no conflicts with the mechanical dimensions of the module. The connectors usually have deviating mechanical pads thus drop-in replacements may require a combined PCB footprint. Please check the manufacturers' datasheets for details.

The recommended connectors for the MPX-T1040 are:

Manufacturer	Type	Board-to-board height	Plating	Comment
JAE	MM70-314B1-2-R300	3mm	0,3µm min. gold plating over Ni	314 pins
Foxconn	AS0B826-S55B-7H	2,7mm	10µm gold plating	
Foxconn	AS0B826-S78B-7H	5mm	10µm gold plating	
Aces	91782-3140M-001	5mm	3µm gold plating	
Amphenol	10151114-001TLF	5mm	30µin gold plating	
Yamaichi	CNU113-314-2201-VE	5mm	0,3µin gold plating	

Table 5-2 Connector Types: Ordering Information

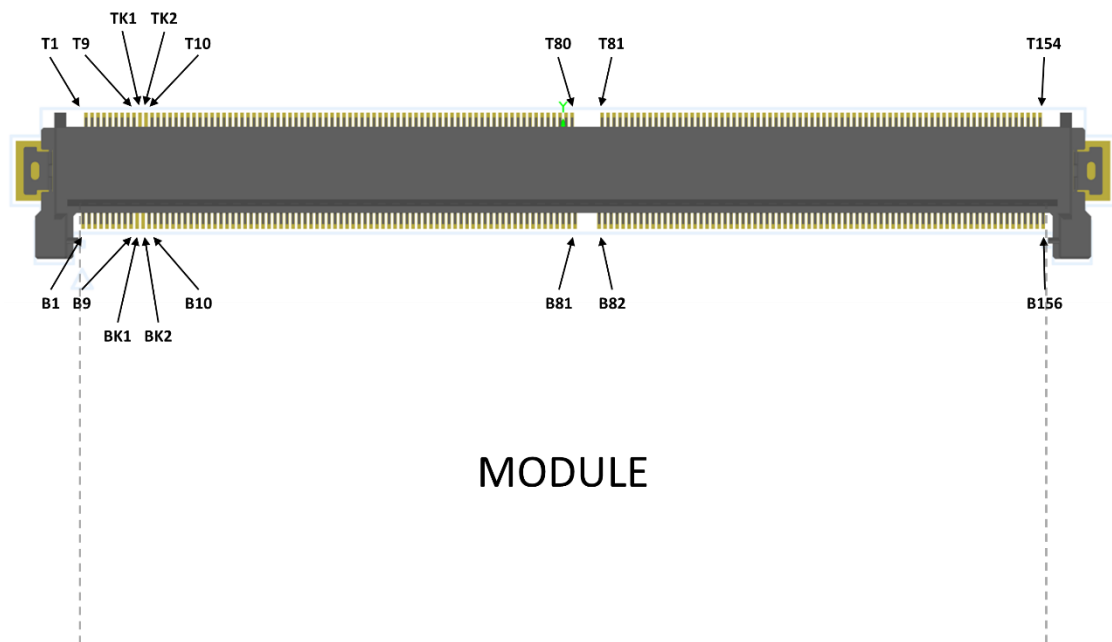


Figure 5-3 Connector pin definition

5.2 Board Outline



For 3D data files please contact MicroSys.

The following drawing shows the mechanical outline (82x62mm) of the MPX-T1042 module plugged in a JAE - MM70-314B1-2-R300 connector. This drawing is not to scale:

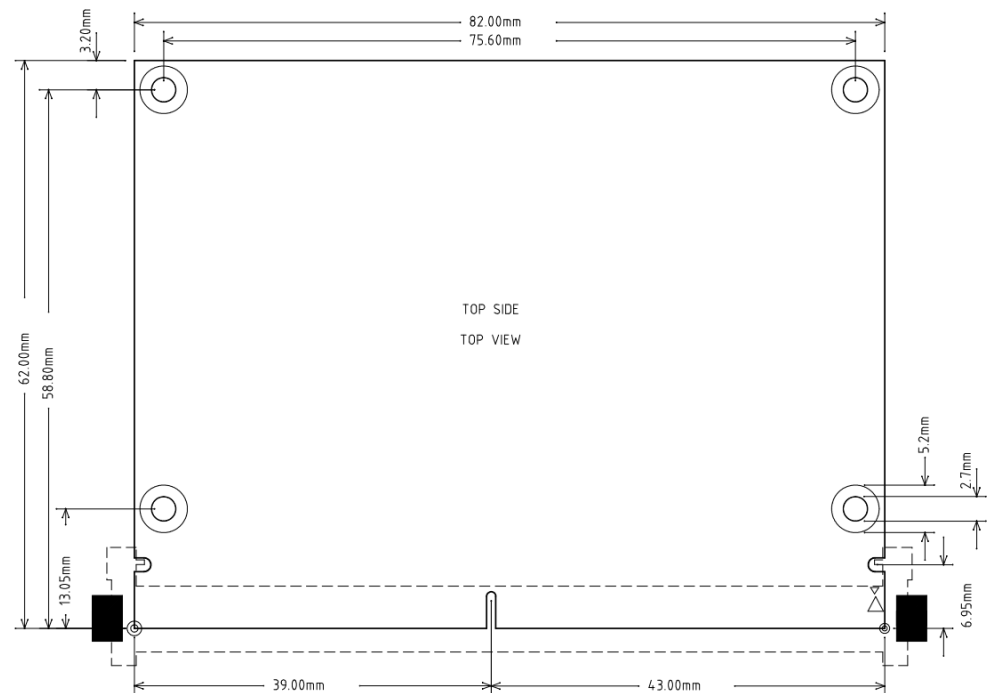


Figure 5-4 Module outline (82x62mm)

The mounting holes can be used with M2.5 screws. Dimensions are designed as follows:

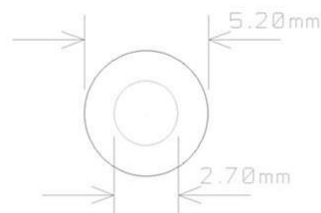


Figure 5-5 Mounting holes: dimensions

5.3 Height

The MPX2 specification defines a maximum constructional height for bottom side parts of MPX2 CPU modules. The height is limited to 2,0 mm including tolerances.

Depending on the connector used, the constructional height for parts on the carrier board placed beneath the module may vary. For example, the MM70 connector with 6,7mm product height allows a total board-to-board height of 3,0 mm. This results in a maximum part height on the carrier board of 1,0 mm.

The MPX-T1042 module conforms with the MPX2 specification.

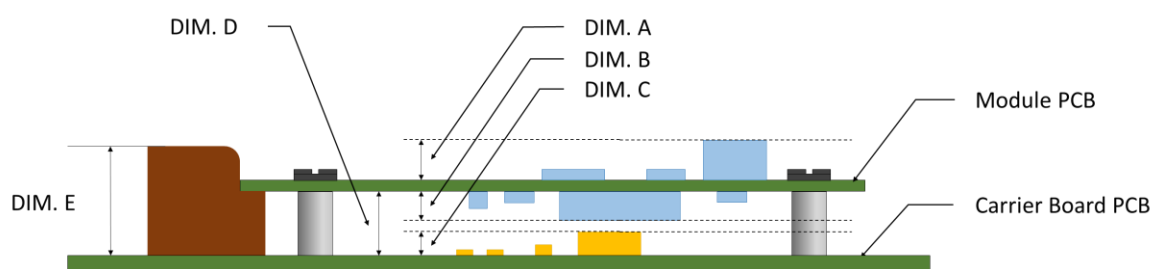


Figure 5-6 Construction height for parts

	Definition	Value	Comment
DIM. A	Module top side parts	4,0 mm	For T1042 modules only
DIM. B	Module bottom side parts	1,6 mm	For T1042 modules only
DIM. C	Carrier board parts under the module	DIM.D minus DIM. B	
DIM. D	Board-to-board height	Depending on connector type	
DIM. E	Connector product height	Depending on connector type	

Table 5-3 Construction height overview

5.4 Thickness

PCB thickness of the MPX-T1042 module is 1,2mm ± 10%.

5.5 Top Side Component Layout

The following table defines the main components on the top side:

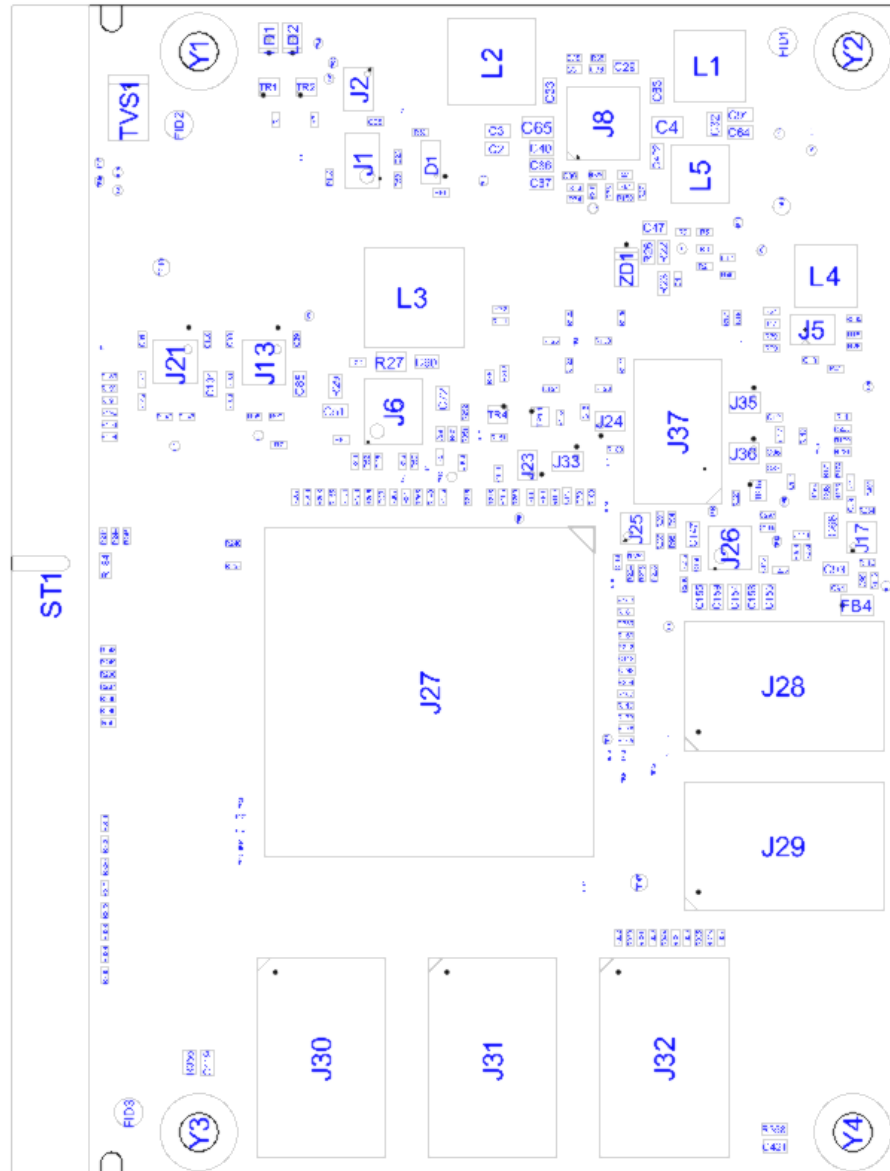


Figure 5-7 Top components

Part Reference	Manufacturer	Type	Function
J27	NXP	T1042	CPU
J28/J29/J30/J31/J32	Micron	MT40A256M16	DDR4 memory
J25	Texas Instruments	TMP451	Temperature sensor
J34	Infineon	S25FL128S	SPI flash
J37	Infineon	CY14V101NA	nvSRAM

Table 5-4 Top side components

5.6 Bottom Side Component Layout

The following table defines the main components on the bottom side:

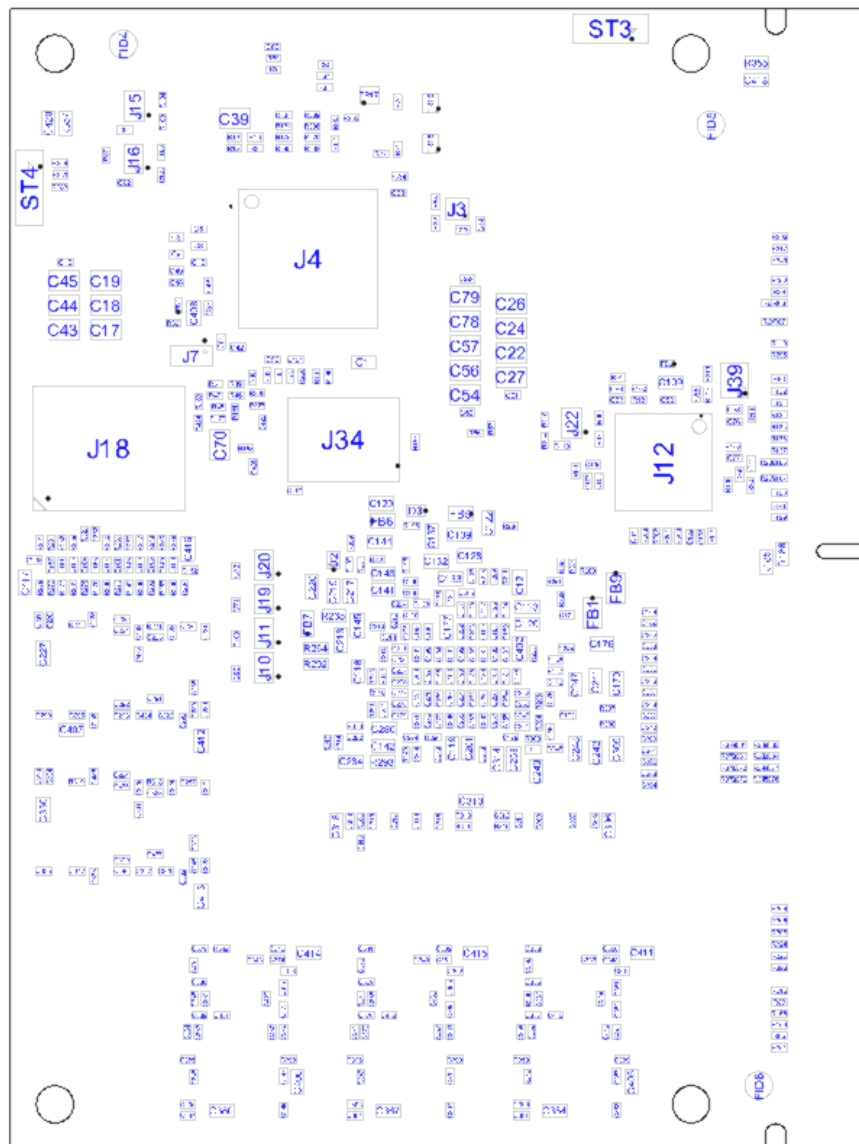


Figure 5-8 Bottom components

Part Reference	Manufacturer	Type	Function
J1	Epson	RX-8803LC	Real-time clock
J2	ST	M24128	EEPROM
J4	NXP	MK02	MCU
J12	IDT	IDT6V49205B	Clock generator
J18	SkyHigh	S34MS04G	NAND flash
ST3	JST	SM06B-XSRS-ETB	Programming connector
ST4	JST	SM06B-XSRS-ETB	Aurora connector

Table 5-5 Bottom side components

6 Software

6.1 U-Boot

The MPX-T1042 uses an U-Boot as standard boot loader, which is always integrated in both the board's NAND and SPI Flash memories on delivery.

Additionally, there's an U-Boot version available to be placed on microSD card if that interface is implemented on the carrier board.

More information on selecting the boot source can be found in chapter 4.2.

The U-Boot carries out the following tasks:

- Pin configuration
- CPU configuration
- Clock configuration
- DDR4 configuration and timing

6.2 Operating System

MicroSys Electronics GmbH offers Linux and Microware OS-9 RTOS support for the module.

Other Operating Systems are available on request only.

7 Safety Requirements And Protective Regulations

7.1 EMC

The System on Module MPX-T1042 is designed according to the requirements of electromagnetic compatibility. Nevertheless, there are several factors which in the target system may require measures against interference.

Active components, especially CPU's of the latest generation do not only operate with high frequencies but also drive very fast signal rise times.

At least the following measures shall be applied:

- Provide sufficient block capacitors in your supply voltages
- Keep short all clock lines in order to prevent interference with other signals
- Shield clock lines with ground planes or keep as much distance as possible to other signals
- provide filtering for all external signals
- provide an EMI proof housing for your electronics

7.2 ESD

For technical reasons there is no ESD protection on the MPX-T1042. Please provide sufficient protection on the baseboard and/or system level.

7.3 Reliability

The SOM MPX-T1042 is available for operation in extended temperature range.

Please note that steady high temperature operation reduces lifetime of all electronic components. Make sure that no component on the module ever exceeds its maximum specified temperature during operation or storage. A reasonable cooling concept can dramatically increase lifetime of your electronics.

The MPX-T1042 is designed to withstand a high level of vibration and shock as there are low weight and no overhanging components on the module. If desired, MicroSys Electronics GmbH can support you with your shock and vibration concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Relevant components on the module are chosen with values for a high level of derating.

7.4 Climatic conditions

The relative humidity during operation or storage of the module may not exceed 10% to 90%, non-condensing.

7.5 RoHS

All components of the MPX-T1042 are RoHS compliant, also a RoHS compliant soldering process is used for manufacturing.

8 General notes

Customers responsibility for chip errata:

It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of.

The manufacturer's advice should be followed.

If desired, MicroSys Electronics GmbH can support you with your lifecycle management regarding to chip errata. Please ask your sales representative or send an email inquiry to support@microsys.de.

9 Appendix

9.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

<i>COP</i>	<i>Common on-chip processor</i>
<i>DIU</i>	<i>Display Interface Unit</i>
<i>DMA</i>	<i>Direct Memory Access</i>
<i>ESD</i>	<i>Electrostatic Discharge</i>
<i>eSDHC</i>	<i>Enhanced Secured Digital Host Controller</i>
<i>GND</i>	<i>Ground</i>
<i>GPIO</i>	<i>General Purpose Input Output</i>
<i>GPL</i>	<i>General Public License</i>
<i>I²C</i>	<i>Inter-Integrated Circuit</i>
<i>LED</i>	<i>Light Emitting Diode</i>
<i>MAC</i>	<i>Media Access Control</i>
<i>MCU</i>	<i>Microcontroller Unit</i>
<i>PU</i>	<i>Pull-Up Resistor</i>
<i>RCW</i>	<i>Reset Configuration Word</i>
<i>RGMI</i>	<i>Reduced Gigabit Media Independent Interface</i>
<i>RTC</i>	<i>Real-Time clock</i>
<i>SATA</i>	<i>Serial Advanced Technology Attachment</i>
<i>SDHC</i>	<i>Secure Digital High Capacity</i>
<i>SerDes</i>	<i>Serializer Deserializer</i>
<i>SGMI</i>	<i>Serial Gigabit Media Independent Interface</i>
<i>SPI</i>	<i>Serial Peripheral Interface</i>
<i>SR</i>	<i>Series Resistor</i>
<i>TDM</i>	<i>Time Division Multiplexing Interface</i>
<i>UART</i>	<i>Universal Asynchronous Receiver/Transmitter</i>
<i>UCC</i>	<i>Universal Communication Controller</i>
<i>USB</i>	<i>Universal Serial Bus</i>

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10 History

Date	Version	Change Description
2017-07-04	1.0	Initial Release Version
2017-08-18	1.1	- Changed Figure 4-1 - Table 4-7: added VREF-MII and VREF-SDC - Table 4-8: added VREF-MII and VREF-SDC; changed direction of TCK signal; added note relating to onboard clocks - Table 4-8 / Table 4-9: added frequencies - Table 4-10: swapped pins T133/T134 - Table 4-17: Direction corrected for TCK, TMS - Table 4-18: PORESET# is connected to Ball F13 - Table 4-39 / Table 4-40 / Table 4-41 / Table 4-44: added VREF-MII - added cross reference to SerDes clock in chapter 4.10.10 - modified Table 5-3
2018-01-26	1.2	- Corrected I/O Level of Pins B125, B130 in Table 4-1 - Added USB-ID I/O Level in Table 4-25, Table 4-26 - UARTx-SIN & UARTx-SOUT re-named UART-RXD & UART-TXD on connector pins in Table 4-29 - Corrected module connector pin for signal "PORESET#" in Table 4-18
2018-02-01	1.3	Added chapter 4.1.4
2018-03-01	1.4	- Revised chapter 5.1 - Revised chapter 5.3
2020-05-18	1.5	JAE connector obsolete: updated Table 5-2
2023-03-01	7.0	Hardware Revision 7 - added nvSRAM in block diagram in chapter 3.1 - updated link to website in chapter 3.5 - added TK1, TK2, BK1, BK2, I2C3 and GPIOs in pin list in chapters 4.1.1 & 4.1.2 - added VCC-PROG-SFP on pin TK2 - removed extension connector (former chapter 4.1.3) - corrected RTC voltage in Figure 4-2 & Figure 4-4 & Table 4-6 - removed former table 4-13 - removed I2C address 0x10 in Table 4-20 - updated SPI-CS0# availability in Table 4-11, chapter 4.5 & 4.10.4 - updated LED chapter 4.6 - updated deviation in chapter 4.7 - temperature sensor exchanged: chapter 4.8 updated - added new chapter 4.9 - added additional GPIOs in Table 4-16 - added I2C3 in Table 4-19 - replaced LM95245 with TMP451 in Table 4-20 - added nvSRAM (chapter 4.10.6) - Chapter 5.1 revised - updated top and bottom side component height in chapter 5.3 - updated chapters 5.5 & 5.6 - PORESET# is connected to F13 (Table 4-5)

Table 10-1 Document history